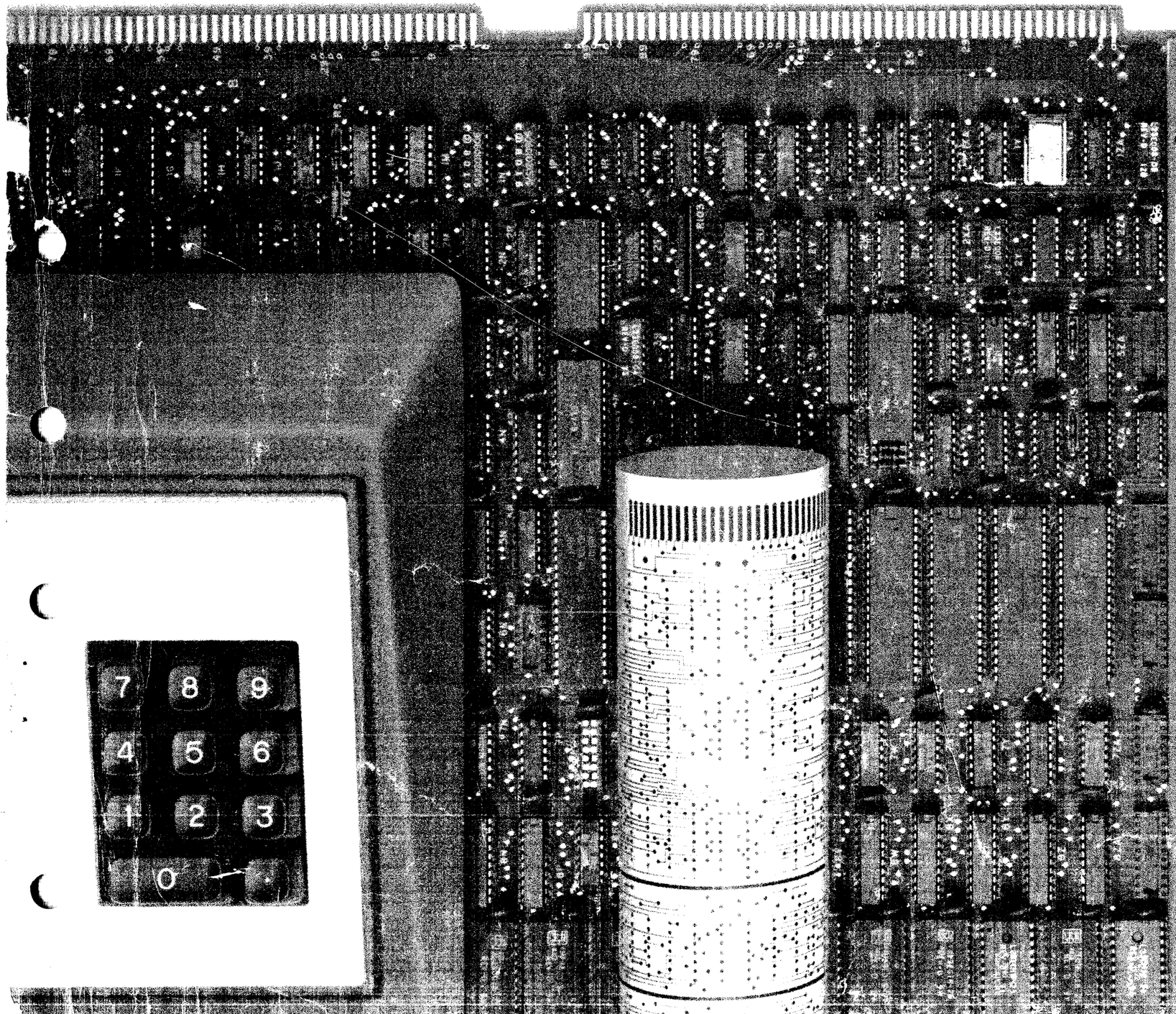
COMPUTERVISION

Technical

Instaview Display

Logic Diagrams



Document control number: 35- 00251

Name _____

Instaview Display Logic Diagrams

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Order No. 001-00535-003

Table of Contents

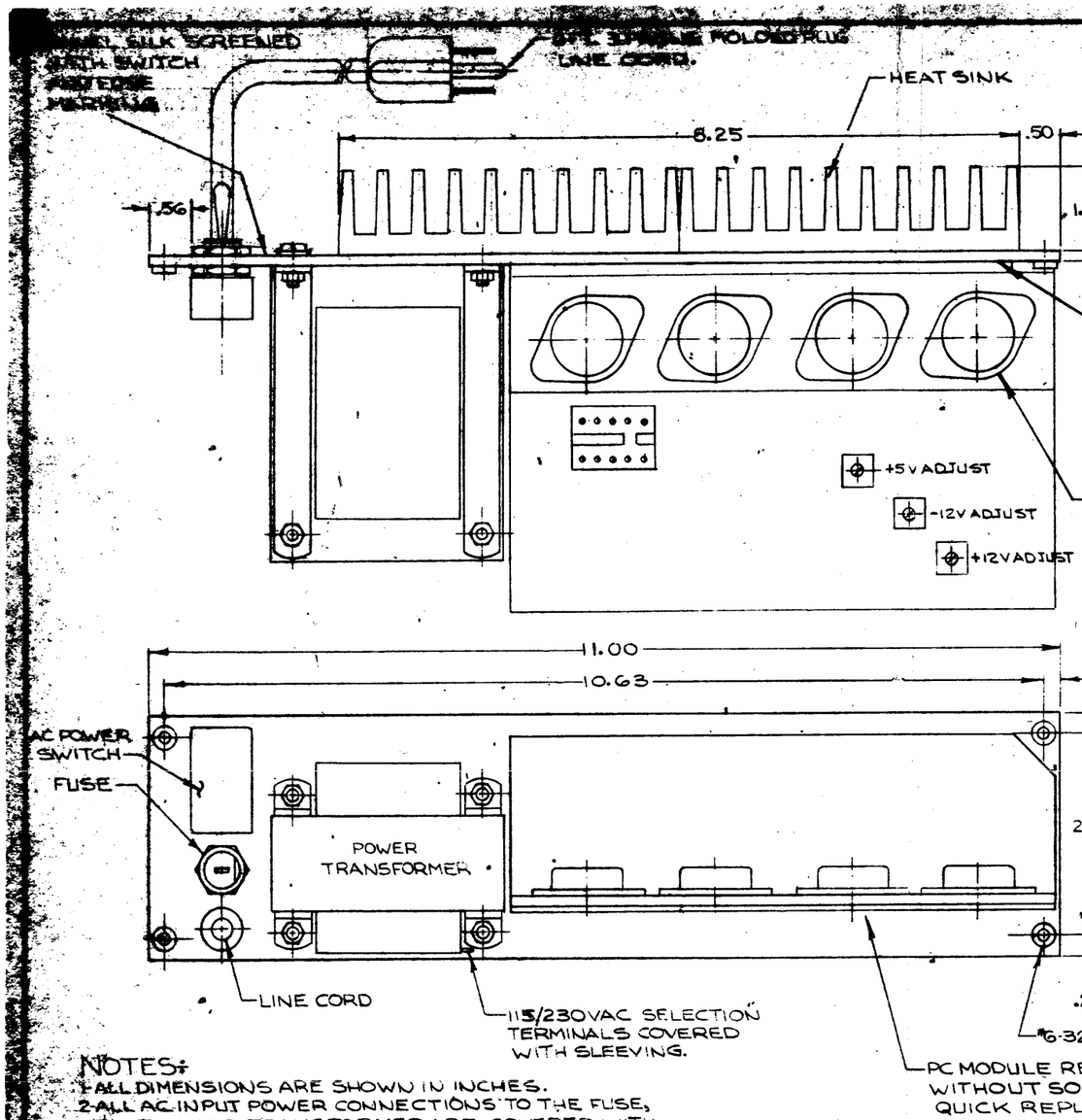
Tablet Power Supply

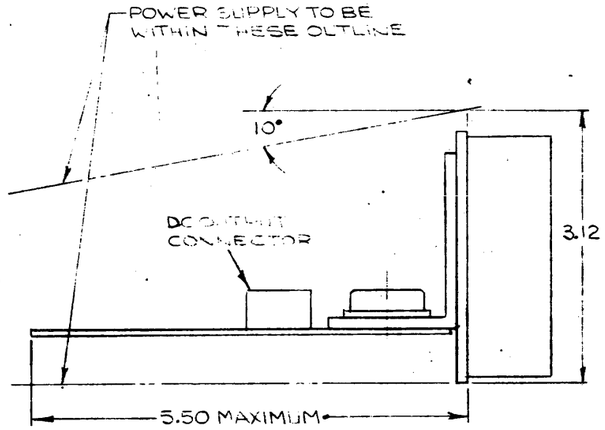
Keltron: Outline and Schematic

Power-One, Inc: Schematic

Power Supply, Incorporated: Schematic

LTR	REVISION	DATE
A	PC MODULE ADDED TO TOP VIEW	6-23-78





NOTES:
1. ALL DIMENSIONS ARE SHOWN IN INCHES.
2. ALL AC INPUT POWER CONNECTIONS TO THE FUSE, SWITCH AND TRANSFORMER ARE COVERED WITH SLEEVING FOR SAFETY PROTECTION.
3. THE DC OUTPUT CONNECTOR IS AN AMP #1-380991-0.
4. THE CONNECTOR PIN ASSIGNMENTS ARE:

1—+5VDC	6—+12VDC
2—+5VDC	7—12V RETURN
3—5V RETURN	8—12V RETURN
4—5V RETURN	9—CHASSIS
5—+12VDC	10—-12VDC

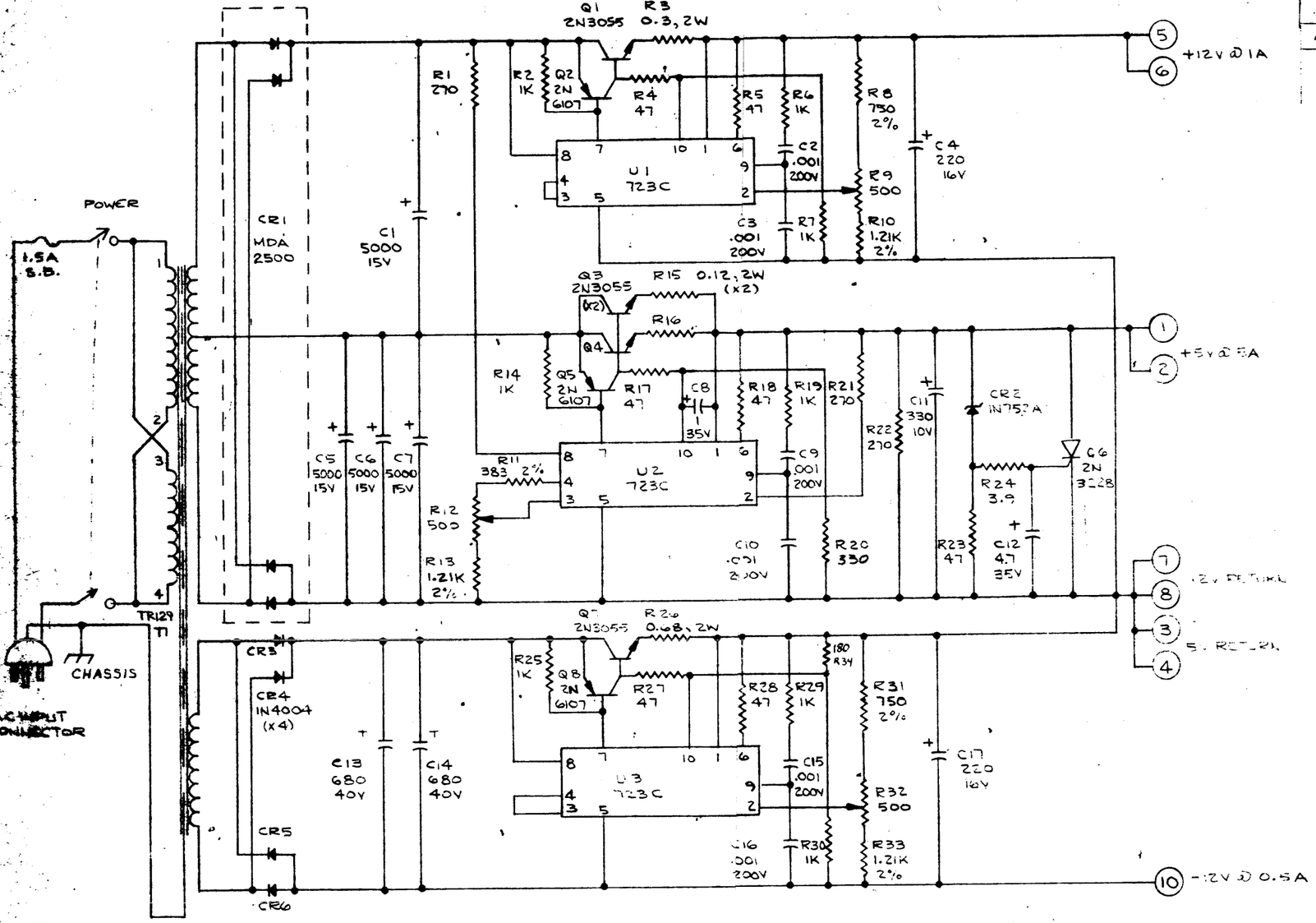
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MACHINE FINISHES
TOLERANCES ON FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
FINISH: BLACK ANODIZE
MATERIAL: ALUM. .12 THK 5052-H32

KELTRON CORPORATION
225 Crescent St., Waltham, Mass. 02154 (617) 894-0525

MODEL MPC3S106 POWER SUPPLY
PROPOSED OUTLINE DRAWING

DR E. WENCEK	CHK	DRAWING NUMBER
DATE 11-22-77	DATE	VC923-001
APPD A.E.S.	SCALE FULL	
DATE 11-22-77		

LTR	REVISION	DATE
1	REMOVE WIRE TO OUTPUT CONNECTOR PIN # 9	2-6-79
2	ADD R34 180 OHM	5-10-79



NOTES:

1. ALL RESISTOR VALUES ARE IN OHMS UNLESS MARKED OTHERWISE.
2. ALL RESISTORS ARE RATED 1/2 W UNLESS NOTED OTHERWISE.
3. ALL CAPACITORS VALUES ARE IN MICROFARADS.
4. FOR 115VAC OPERATION, THE PRIMARY WINDINGS ARE CONNECTED IN PARALLEL WITH A JUMPER FROM TRANSFORMER PIN # 1 TO PIN # 3 AND AN OTHER JUMPER FROM PIN # 2 TO PIN # 4.
5. FOR 230VAC OPERATION, THE PRIMARY WINDINGS ARE CONNECTED IN SERIES WITH A JUMPER FROM TRANSFORMER PIN # 2 TO PIN # 3.

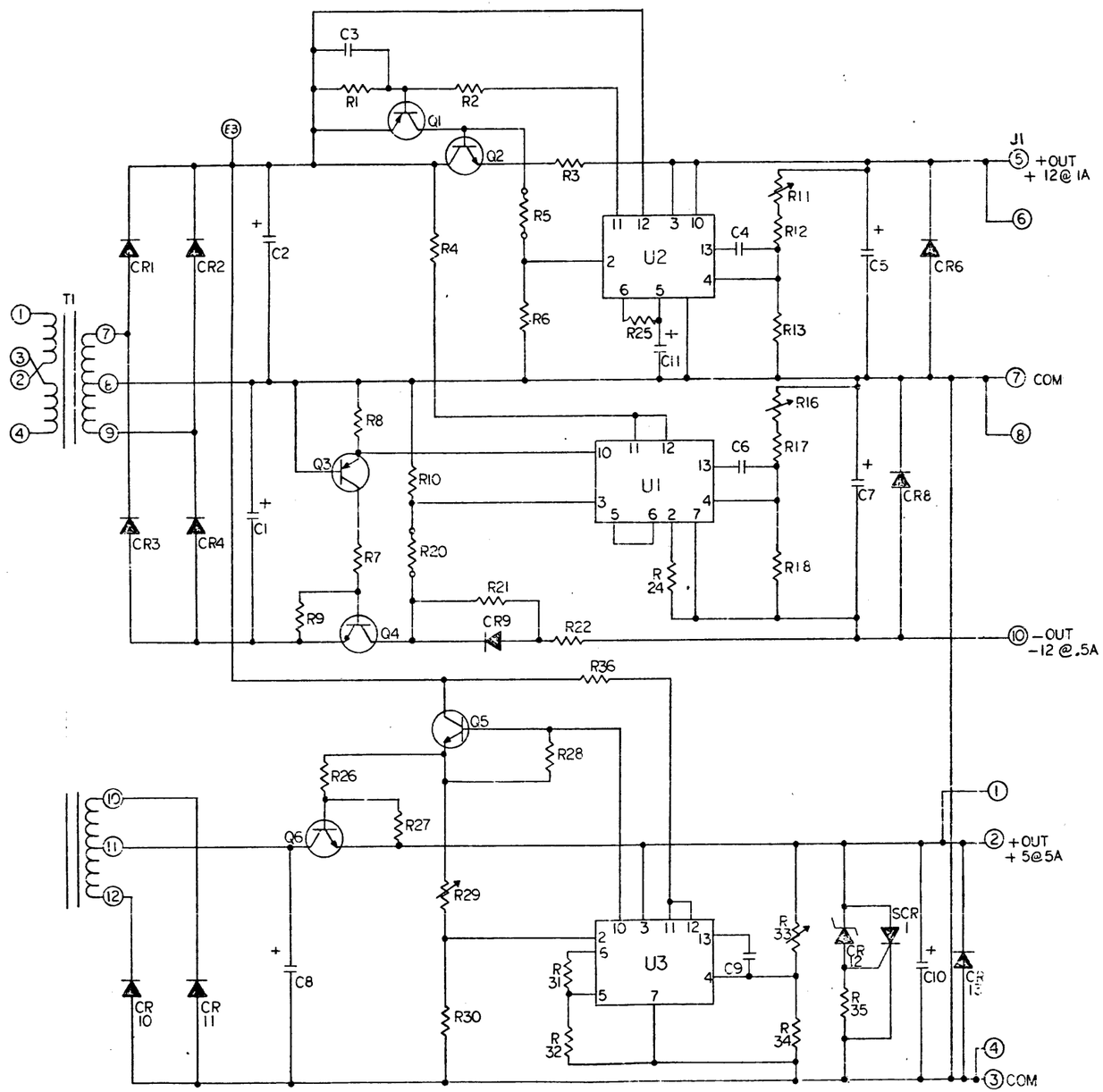
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
MACHINE FINISHES ✓
TOLERANCES ON
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
FINISH:
MATERIAL:

KELTRON CORPORATION

MODEL MPC 35106 POWER SUPPLY SCHEMATIC DIAGRAM

DR J.P.	CHK W.E. LORDER	DRAWING NUMBER
DATE 23 MAY 78	DATE 6-7-78	VC923-501
APPD	SCALE	
DATE		

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROTO CLEAN-UP	2/21/79	J.F.
	B	ADDED J1	8-13-79	K.C.
2274	C	R82 WAS 151-10411	10/22/79	KC.
2541	D	ADDED NOTE TO SCHEMATIC #16113	12-13-79	K.C.
4438	E	ADDED HARDWARE LIST	1-14-81	KCS.



C1, 2	2200/35	CAPACITOR ALUM ELECT	102-10100
C3			
C5, 7	100/35		101-10110
[2] C8	16000/15		102-10096
C10	220-16		101-10107
C11	1/50	ALUM ELECT	101-10111
C4	.001/100	MYLAR	104-10093
C6	.003-100		104-10092
C9	.01/100	CAPACITOR MYLAR	104-10095
CR1,2,3,4,6,8,9	AE1C	DIODE 1A 200V	111-10251
CR10, 11	MR750	22A 50V	111-10256
CR12	IN752A	ZENER	112-10006
CR13	AF3B	DIODE 3A 100V	111-10252
SCR1	S0508LS3	SCR 50V 8A	160-10013
Q1, 3	2N2907A	TRANSISTOR	172-10248
→ Q2, 4	12500-3		171-10261
→ Q6	12505-2		171-10262
Q5	2N6551	TRANSISTOR	172-10249
U1, 2, 3	Lin 723	IC VOLTAGE REGULATOR	130-10287
R1	1.6K	RESISTOR ½W 5% CF	151-10370
R2, 5, 7, 8, 20, 36	330Ω		151-10353
R4	750Ω		151-10362
R6, 9, 10	4.7K		151-10381
R17, 12	150Ω		151-10345
R24	47Ω		151-10333
R21	1.5Ω		151-10302
R26	2.7Ω		151-10305
R27	22Ω		151-10325
R28	2.2K		151-10373
R25	470Ω		151-10357
R30	3.9K		151-10379
R35	82Ω	½W 5% CF	151-10339
R13, 18	1.2K	½W 2% MF	152-10507
R32, 31	2.4K		152-10514
R34	2K	½W 2% MF	152-10512
R3, 22	.56Ω	2W 10% BWH	158-10082
R11, 16, 33, 29	2K	RESISTOR POTENTIOMETER	154-20020
J1	1-380991-0	CONNECTOR AMP	901-10823
T1	16116	TRANSFORMER	082-16116
P C B	16117	PRINTED CIRCUIT BOARD	505-16117
CHASSIS	16114	CHASSIS	412-16114

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	STD P/N

PARTS LIST

QTY	STD. P/N	DESCRIPTION	USED ON
2	360-20018	SLEEVING, 18GA, 7/8"	C8+, C8-
1	350-10663	SCREW 6-32 X1"	SCR1
1	402-13920	HEATSINK	SCR1
2	321-10679	I.C. SOCKET, 14 PIN	U1, U2

HARDWARE LIST

LAST REFERENCE DESIGNATION USED			
C 10	CR 13	Q 6	R 35
SCR 1	T 1	U 3	E 3
J 1			

NOT USED
R14, R15, R19, R23, CR5, CR7
E1, E2

NEXT ASSY	USED ON
	CP331

APPLICATION

NOTES:
1. RTV LARGE CAPS TOGETHER ON BOARD.

TOLERANCE .XX = .030
.XXX = .010

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN L. FOORMAN	2-12-79
CHECKED	
ENG. APP.	
APPROVED	

POWER-ONE, INC.
CAMARILLO, CALIF. 93010 (805)484-2806

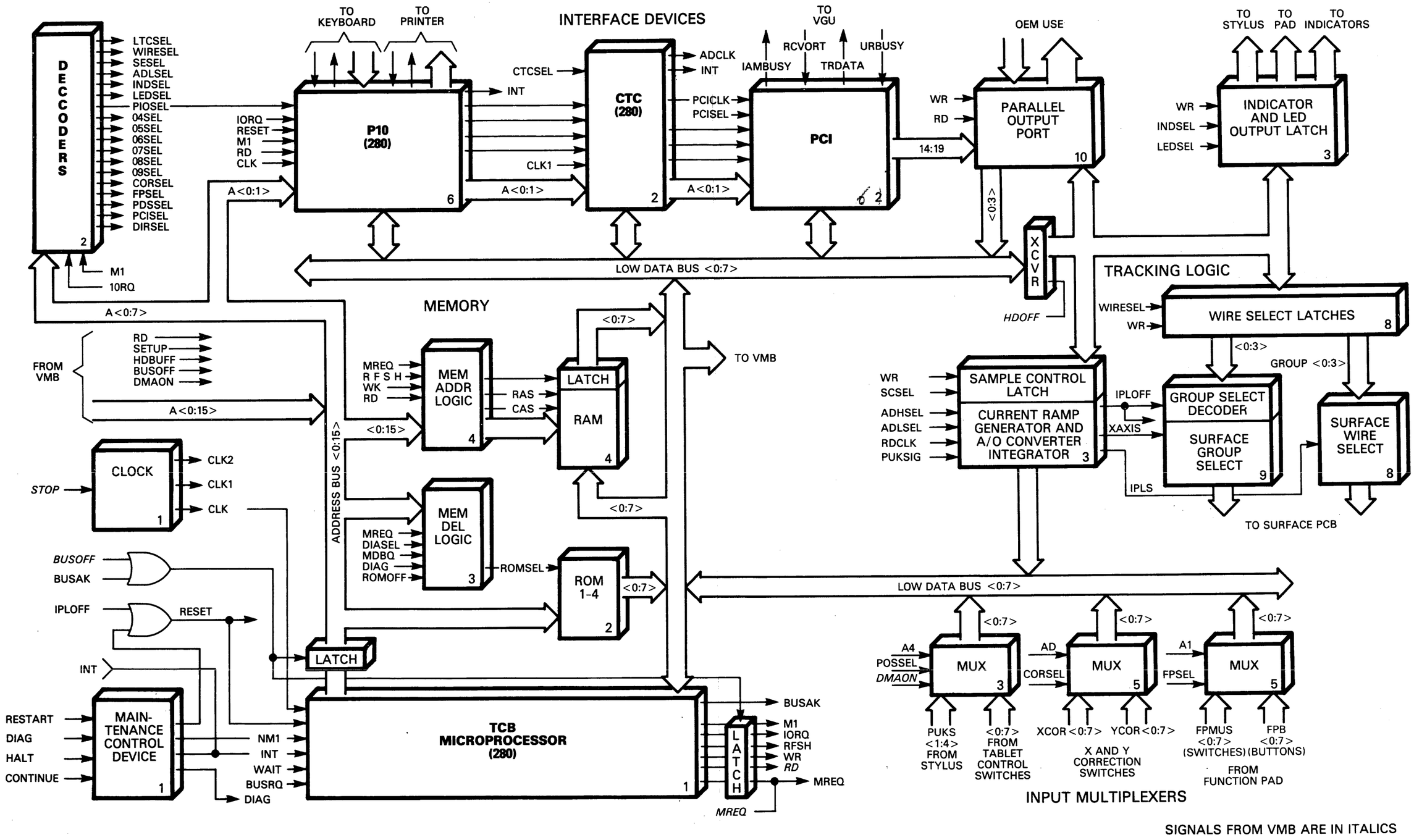
TITLE: SCHEMATIC

SIZE	CODE IDENT NO.	DRAWING NO.	
D	54407	16113	E

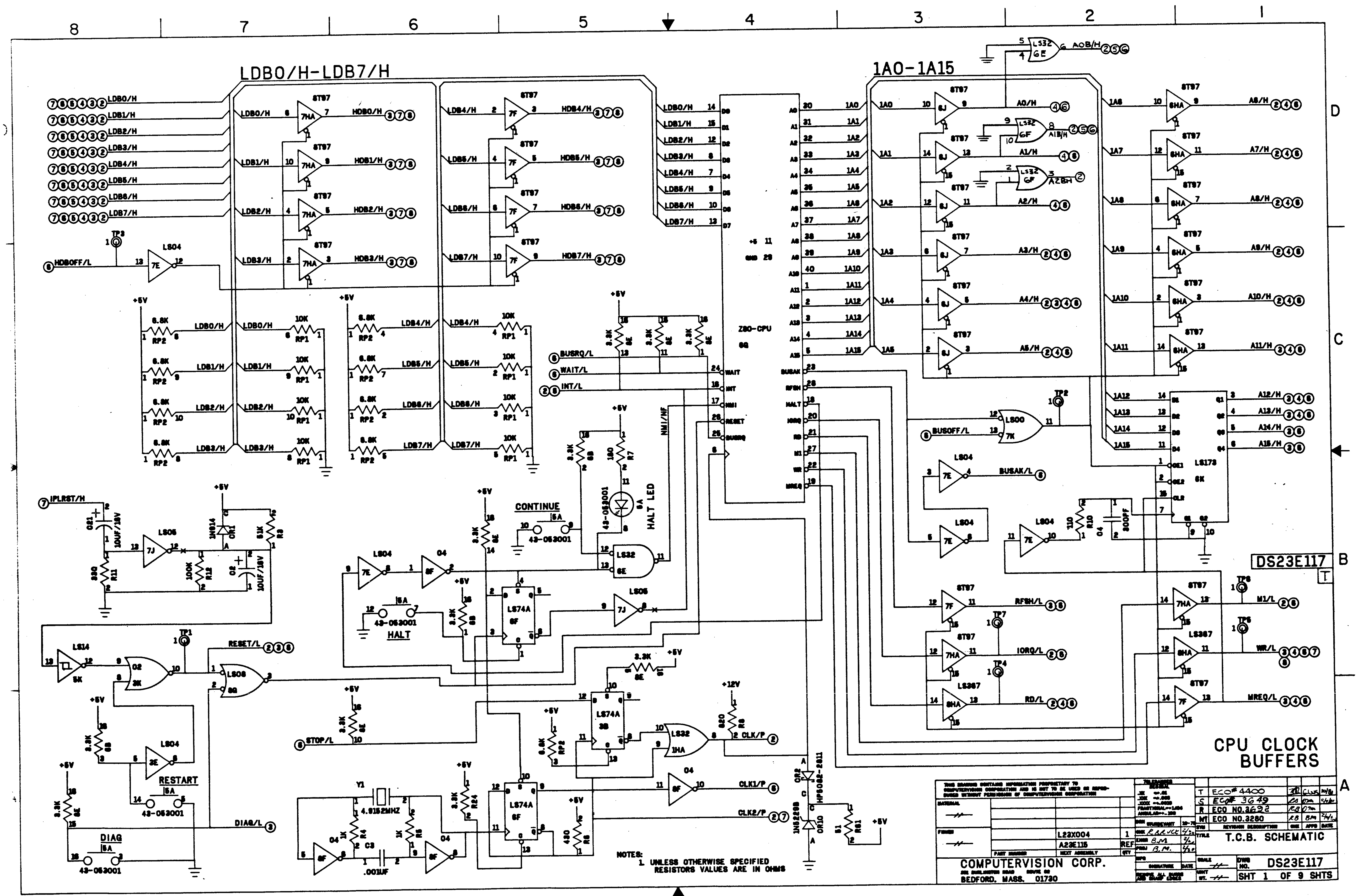
SCALE — SHEET / OF /

BISHOP GRAPHICS/ACCUPRESS RECORDER NO A-1540

Tablet Controller Board



Tablet Controller Board Simplified Block Diagram



LDB0/H-LDB7/H
1A0-1A15
Z80-CPU
CONTINUE
HALT
HALT LED
RESTART
DIAG
STOP/L
RESET/L
CLK/P
CLK1/P
CLK2/P
4.9152MHZ
DS23E117
CPU CLOCK
BUFFERS
NOTES:
1. UNLESS OTHERWISE SPECIFIED
RESISTORS VALUES ARE IN OHMS
ECO# 4400
ECO# 3649
ECO NO.3692
ECO NO.3280
L23X004
A23E115
T.C.B. SCHEMATIC
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DS23E117
SHT 1 OF 9 SHTS

8 7 6 5 4 3 2 1

D C B A

2A0-2A7

J3-KEYBOARD

J2-PRINTER

LDB0/H-LDB7/H

2B0-2B7

Z80-PIO 4C

Z80-CTC 3H

2518 4E

2518 4F

2518 4H

2518 4G

LS138 1E

LS138 2E

LS138 2F

LS138 3F

LS367

LS04

LS08

LS10

LS21

LS27

LS00

330 R60

470PF C60

2.2K R68

TP18

AOB/H-AZB/H

DS23E117

I/O DEVICE DECODING,ROMS. KEYBOARD/PRINTER INTERFACE. CTC SCHEMATIC

T.C.B. SCHEMATIC

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

SEE SHEET 1

SHT 2 OF 9 SHTS

TABLET CONTROL SWITCHES

+5V

8.2K 7B

DIP SW 8A

J8 9 PUKS2/L

J8 18 PUKS1/L

J8 20 PUKS3/L

J8 19 PUKS4/L

LS257A 8C

LDB0/H LDB1/H LDB2/H LDB3/H

J8 22 GND

J8-PEN/PUCK

LS257A 8B

LDB4/H LDB5/H LDB6/H LDB7/H

J8 23 PUKS5/L

DMAON/H

A4/H

PDSSEL/L

HDB0/H-HDB7/H

LS377 9D

LS377 9C

FPD1/L FPD2/L FPD3/L FPD4/L PUKD1/L PUKD2/L PUKD4/L

J8 8 J8 7 J8 10

LEDSEL/L

WR/L

INDSEL/L

J8-PEN/PUCK

LS05 7J

R64 8.2K

10P CNB-06

BUZZER

+5V TP28 C48 10UF/16V

J4 2 J4 20 J4 8 GND J4 26

J4- IMAGE CONTROL UNIT

436733-7 9AA

INDICATOR LEDS

+5V TP29 TP33

J10-POWER

J10 1 J10 2 GND J10 3 J10 4 +12V J10 5 J10 6 AGND J10 7 J10 8 -12V J10 10

TP28 TP31 TP32 TP40 TP42 TP43 C25 10UF/16V

TP24 TP26 C26 10UF/16V

TP25 TP30 TP36 C27 10UF/16V

ROMOFF/L

MREQ/L

A13/H

A14/H

A15/H

RFSH/L

LS27 1H

S04 1K

LS00 3B

LS08 8B

G2 2K

CR9 1N914

430 R49

C30 .0047F

RAMSEL/L

A11/H

A12/H

LS139 2F

ROM2SL/L ROM3SL/L

RESET/L

HDB0/H

DIASEL/L

DIAB/L

LS74A 2K

LS32 1HA

LS08 2B

ROM4SL/L ROM1SL/L

TP13 TP14 TP15 TP12

PWR CONN.MEMORY DECODING LOGIC.
PUCK SWITCH TABLET CONTROL SWITCH INPUTS.
INDICATOR.PUCK.FUNCTION PAD LED OUTPUT LATCHES

DS23E117

T

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

SEE SHEET 1

T.C.B. SCHEMATIC

DWG NO. DS23E117

SHT 3 OF 9 SHTS

A0/H-A13/H

4A0-4A6,CAS/N,WR/L,AND RAS/N

A7/H A0/H A8/H A1/H A9/H A2/H A10/H A3/H → S257 8J → 4A0 4A1 4A2 4A3

A11/H A4/H A12/H A5/H A13/H A6/H → S257 8K → 4A4 4A5 4A6

+5V → 2.2K R86

32 8M → CAS/N

WR/L
RAS/N
RD/L
RAMSEL/L
MREQ/L

32 8M → 330 R1 → 100PF C1

+12V FOR RAMS → C81 10UF/16V

-12V → C88 10UF/16V → 96 LM320MP-5 -5V REG → C89 10UF/16V → TP26 → -5V FOR RAMS

4A0 4A1 4A2 4A3 4A4 4A5 4A6 CAS/N WR/L RAS/N → 4116 8K

C36 +12V .033UF
C35 +5V .033UF
C37 -5V .033UF

LS367 8HA

4A0 4A1 4A2 4A3 4A4 4A5 4A6 CAS/N WR/L RAS/N → 4116 8J

C38 +12V .033UF
C39 -5V .033UF

LS367 8HA

4A0 4A1 4A2 4A3 4A4 4A5 4A6 CAS/N WR/L RAS/N → 4116 8HA

C34 +12V .033UF
C43 -5V .033UF

LS367 8HA

4A0 4A1 4A2 4A3 4A4 4A5 4A6 CAS/N WR/L RAS/N → 4116 8H

C40 +12V .033UF → DM8097 8H → LDB4/H
C41 -5V .033UF → DM8097 8H → LDB5/H
C42 +12V .033UF → DM8097 8H → LDB6/H
C43 -5V .033UF → DM8097 8H → LDB7/H

LDB0/H
LDB1/H
LDB2/H
LDB3/H

DS23E117 B T

16K RAM

MATERIAL
FINISH
SEE SHEET 1
PART NUMBER NEXT ASSEMBLY QTY

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

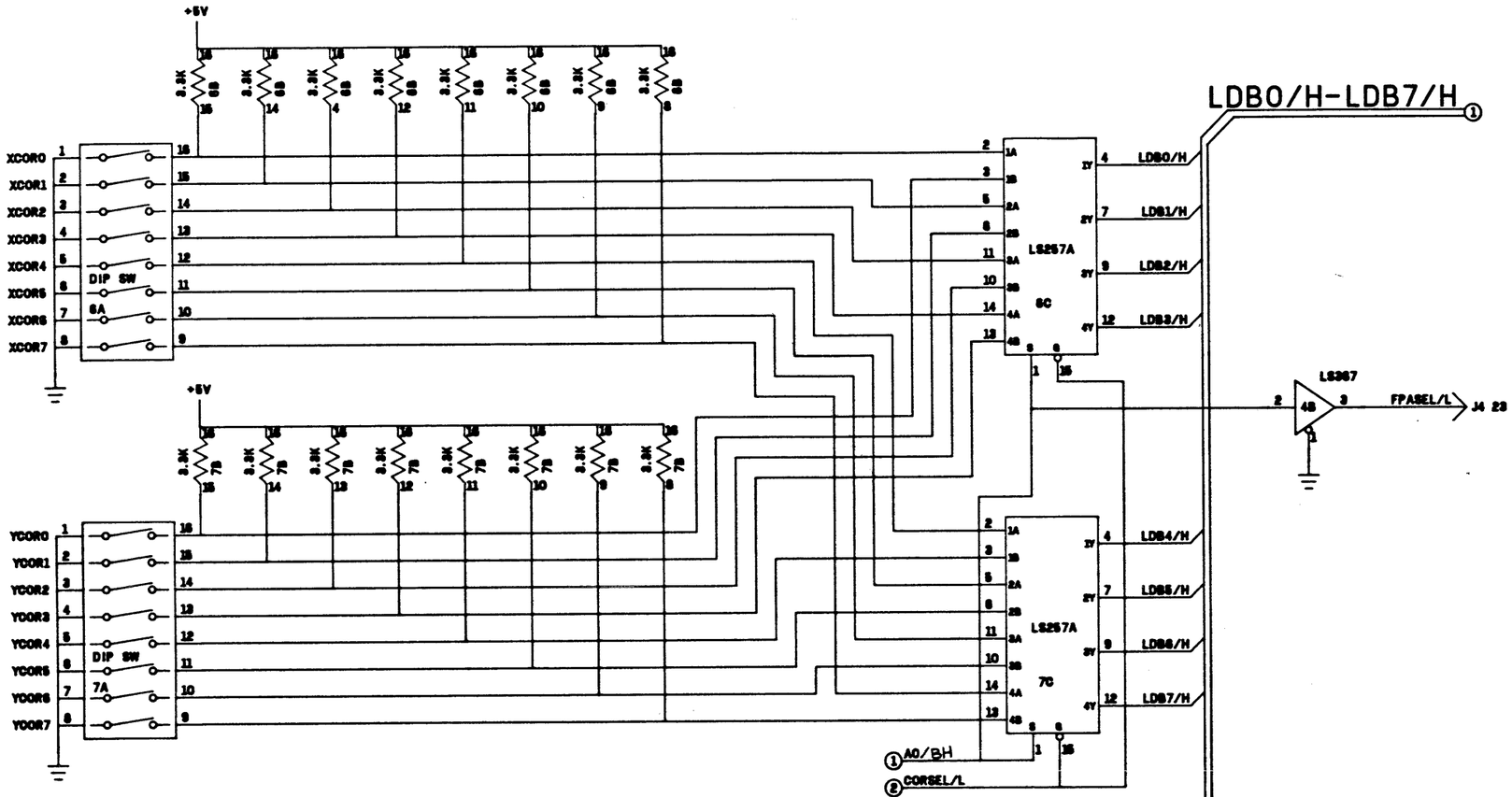
DRAWN STRUKHOFF 20-76
CHK
ENGR
PROJ
APPD
DATE
SIGNATURE

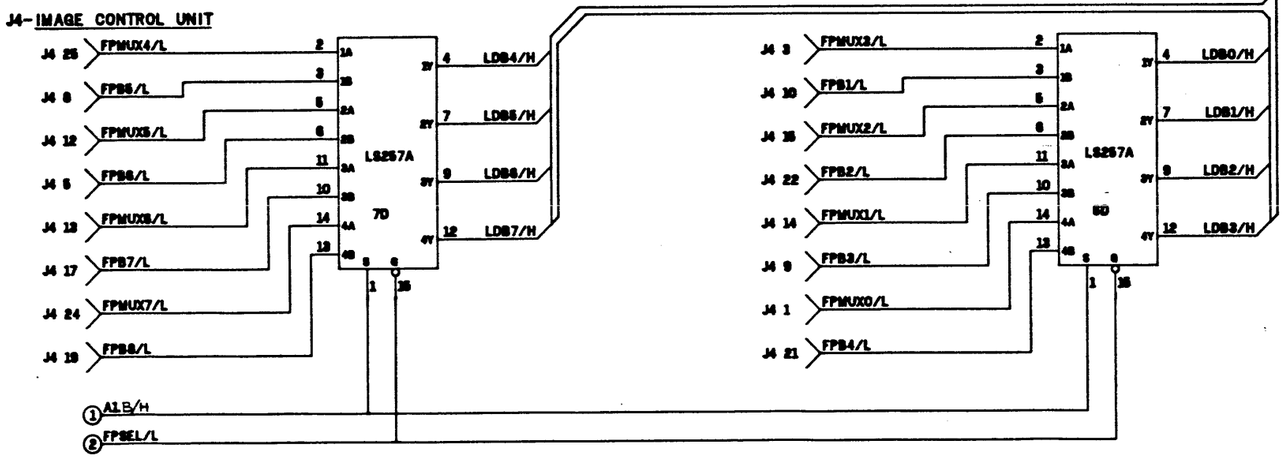
SEE SHEET 1

REVISION DESCRIPTION	ECO	APPD	DATE

TITLE T.C.B. SCHEMATIC

SCALE
DWG NO. DS23E117
SHT sz. SHT 4 OF 9 SHTS





DS23E117

IMAGE CONTROL UNIT INPUTS
X AND Y CORRECTION SWITCH INPUTS

SEE SHEET 1

COMPUTERVISION CORP.
201 BURLINGTON ROAD BLDG. 60
BEDFORD, MASS. 01730

T.C.B. SCHEMATIC

DWG NO. DS23E117

SHT 5 OF 9 SHTS

J5-VGU

J5 7 RCVDAT+ — 51 R16 — 4N37 9AB

J5 19 RCVDAT-

J5 18 URBUSY+ — 51 R15 — 4N37 9AC

J5 5 URBUSY-

+5V — 5.1K R14, 5.1K R13

LS14 5K — LS14 5K — LS14 5K — 804 1K

LS74A 2K

RESET/L → J7 45

.01U .033UF

J5 25 RES1A — 75 R19

J5 8 RES1B

J5 22 RES2A — 75 R20

J5 11 RES2B

J5 9 RES3A — 75 R21

J5 24 RES3B

J5 13 RES4A — 75 R22

J5 20 RES4B

J5 4 KEY

100K R86, 100K R86

LS00 2K — LS00 2B

A1B/H

A0B/H

RESET/L

LDB0/H-LDB7/H

LDB0/H LDB1/H LDB2/H LDB3/H LDB4/H LDB5/H LDB6/H LDB7/H

2651-PCI 8L

THRMT THRDY TXD STB RXRDY RXD RTS DB0 DB1 DB2 DB3 DB4 DB5 DB6 DB7 DBIN DTR R/W RESET A0 A1 BRCLK CS

+5V — 8.2K R50

LS74A 7M

TP8

PCICLK/P

TP10 — DM8097 8H

TP9 — DM8097 8H

+5V — 1N914 CR3, 1N914 CR4, 110 R17, 110 R18

J5-VGU

TRDATA+ J5 14

TRDATA- J5 2

IAMBUSY+ J5 3

IAMBUSY- J5 16

+5V — 8.2K 8E, 8.2K 8E, 8.2K 8B, 8.2K R9

J7-VMB

BUSOFF/L J7 26

DMAON/H J7 34

HDBOFF/L J7 44

ROMOFF/L J7 49

BUSAK/L J7 29

WAIT/L J7 47

.033UF C20, .033UF C18

J7-VMB

J7 41 GND J7 43 J7 27 J7 31 J7 33 J7 35 J7 36 J7 39

TP41

M1/L J7 28
IORQ/L J7 30
RFSH/L J7 32
INT/L J7 37
CLK1/P J7 38
MREQ/L J7 46
STOP/L J7 48
BUSRQ/L J7 50

LDB0/H J7 1
LDB1/H J7 2
LDB2/H J7 3
LDB3/H J7 4
LDB4/H J7 5
LDB5/H J7 7
LDB6/H J7 8
LDB7/H J7 9

WR/L → J7 40

RD/L → J7 42

PCISEL/L

A0/H-A15/H

J7-VMB

A0/H J7 10, A1/H J7 12, A2/H J7 11, A3/H J7 13, A4/H J7 14, A5/H J7 15, A6/H J7 16, A7/H J7 17

A8/H J7 18, A9/H J7 19, A10/H J7 20, A11/H J7 21, A12/H J7 22, A13/H J7 23, A14/H J7 24, A15/H J7 25

DS23E117 B T

VGU INTERFACE
VMB CONNECTOR

UNLESS OTHERWISE SPECIFIED: .XX +-.01, .XXX +-.005, .XXXX +-.0050, FRACTIONAL +-1/64, ANGULAR +-.5DG

MATERIAL — FINISH — NEXT ASSEMBLY — SEE SHEET 1 — QTY

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

DRAWN — CHECKED — ENGR — PROJ — MFG — SIGNATURE — DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHEET 1

DWG	REVISION DESCRIPTION	ECO	APPD	DATE

TITLE: T.C.B. SCHEMATIC

SCALE — DWG NO. DS23E117

SHT WT. — SHT 6 OF 9 SHTS

CURRENT RAMP GENERATOR A/D CONVERTER

DS23E117

T

INTEGRATE AND HOLD

D/A CONVERTER

ADB0/H-ADB9/H

LDB0/H-LDB7/H

(30 U SEC)

(12.8 U SEC ONE SHOT)

SAMPLE CONTROL LATCH

CURRENT RAMP GENERATOR

CURRENT DETECT COMPARATOR

CURRENT PULSE ERROR F/F

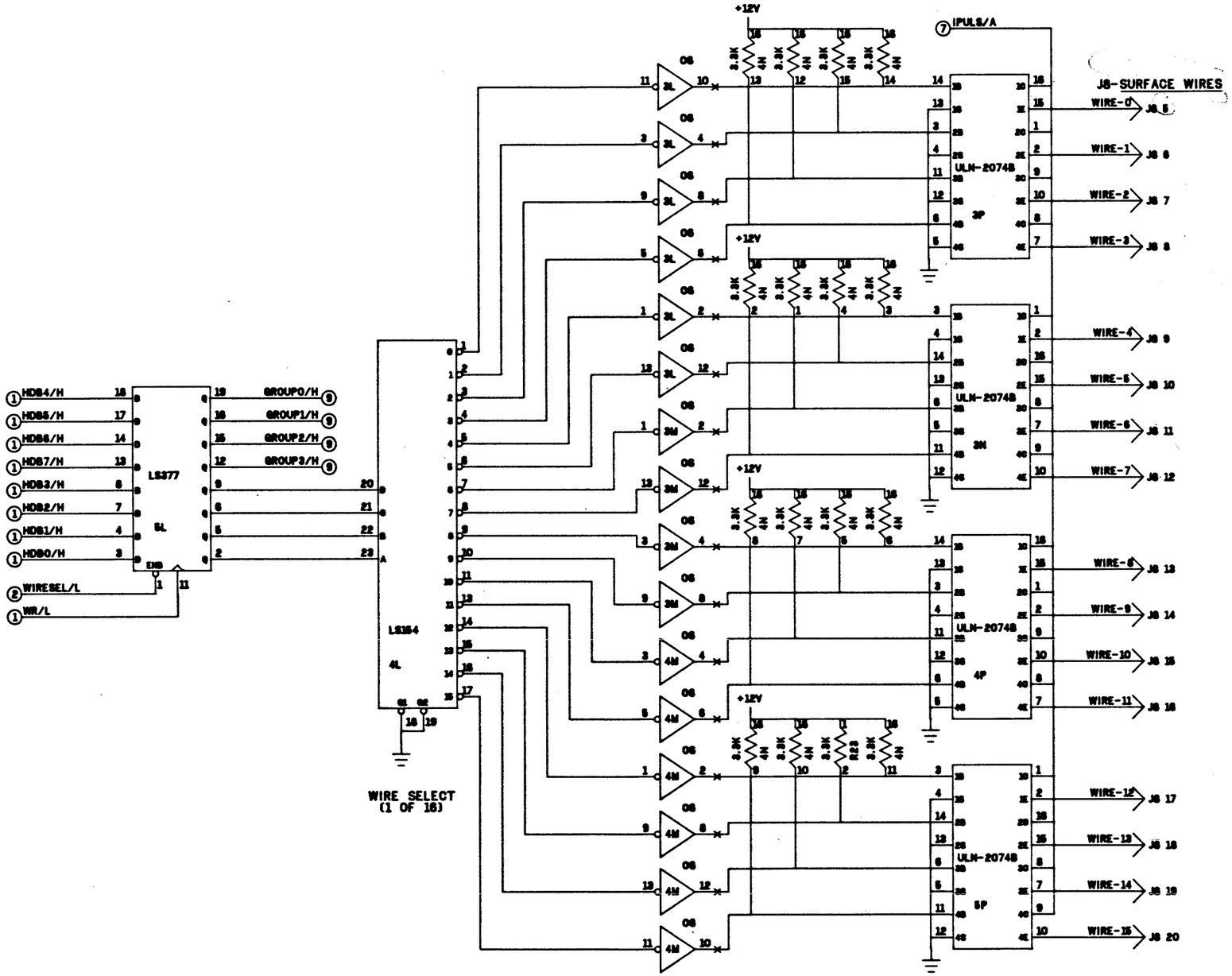
HEAT SINK

J6-PEN/PUCK

DWG NO.	DS23E117
SHT	7 OF 9 SHTS
TITLE	T.C.B. SCHEMATIC
SCALE	
UNIT	

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

SEE SHEET 1



DS23E117
T

SURFACE WIRE SELECT

SEE SHEET 1

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

SEE SHEET 1

T.C.B. SCHEMATIC

DWG NO. DS23E117

SHT 8 OF 9 SHTS

SURFACE GROUP SELECT

GROUP3/H
GROUP2/H
GROUP1/H
GROUP0/H
IPLOFF/H
XAXIS/L
LS154
2L
LS240
ULN-2003A
1K RP6
1K RP4
1K RP9
430 R80
430 R81
430 R82
430 R83
+5V
2N3906 Q4
2N3906 Q5
J9-SURFACE GROUPS
X=0 J9 26
X=1 J9 13
X=2 J9 25
X=3 J9 12
X=4 J9 24
X=5 J9 11
X=6 J9 23
X=7 J9 10
X=8 J9 22
X=9 J9 9
X=10 J9 21
X=11 J9 8
Y=0 J9 1
Y=1 J9 14
Y=2 J9 2
Y=3 J9 15
Y=4 J9 3
Y=5 J9 16
Y=6 J9 4
Y=7 J9 17
Y=8 J9 5
Y=9 J9 18
Y=10 J9 6
Y=11 J9 19

DS23E117

SEE SHEET 1

COMPUTERVISION CORP.
BEDFORD, MASS. 01730

T.C.B. SCHEMATIC

DWG NO. DS23E117

SHT 9 OF 9 SHTS

TCB SIGNAL GLOSSARY

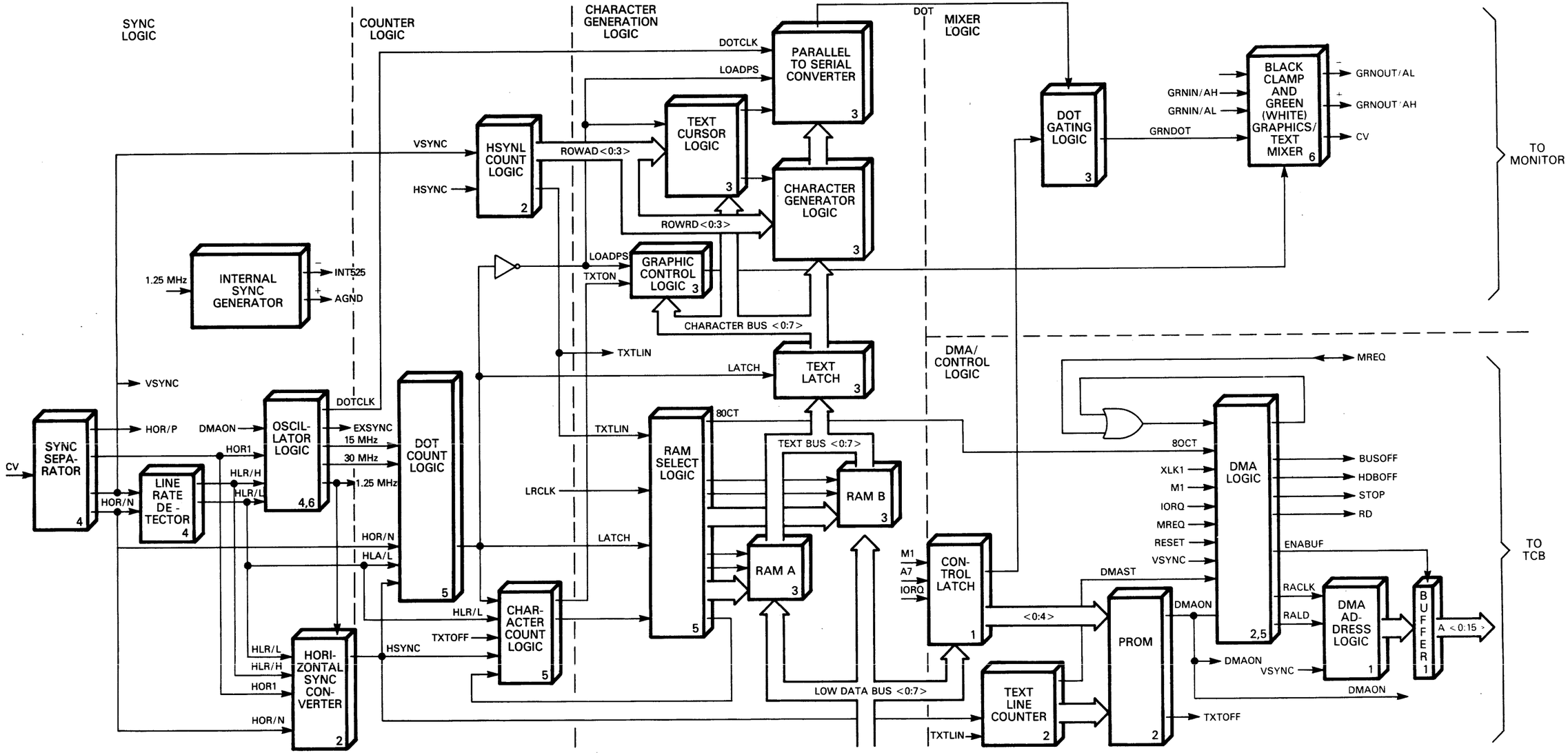
ADB0:ADB9	Analog-to-digital bits — carries analog-to-digital converter data to low data bus.
ADCLK/P	Analog-to-digital clock — from Z80-CTC; derived from system clock (CLK/P) to clock successive approximation register (approximately 1.25 MHz).
ADST/N	Analog-to-digital start — start pulse for analog-to-digital converter; conversion begins after rising edge.
ADHSEL/L	Analog-to-digital converter high byte select — from I/O decoder to enable the high byte of the analog-to-digital converter onto the low data bus.
ADLSEL/L	Analog-to-digital converter low byte select — from I/O decoder enabling analog-to-digital converter to send the pen location information (low byte of analog-to-digital converter) onto the low data bus to the CPU.
A0:A15/H	Address 0:15 — address bus from CPU that is used for addressing. 0:15 are used for addressing the RAM; 0:10 for addressing the ROM; 11 and 12 for selecting the ROM; and 0:7 for addressing I/O devices.
BUSAK/L	Bus acknowledge — from TCB CPU to indicate to the requesting device that the address bus, data bus and control signals are at a high-impedance state and able to be controlled by the requesting device.
BUSOFF/L	Bus off — forces address bus, data bus, and control signals to a high-impedance state so that an external device can take control of them. Used by the VMB direct memory access circuitry to grab bytes from the TCB RAM.
BUSRQ/L	Bus request — from device to CPU to request that the address bus, data bus and control signals go to a high-impedance state so that the device can control them.
BUSY/L	Busy — from CPU (HDB2) to indicate that coordinate data at the parallel output latches is not ready.
CAS/N	Column address strobe — from gated RAMSEL and MREQ signals (+30ns delay) to strobe column address from memory address multiplexer into RAM.
CC/L	Conversion complete — from successive approximation register to LDB6 to indicate that the analog-to-digital conversion is complete.
CLK/P	Clock — from crystal oscillator to CPU and PIO to synchronize internal operations (frequency is 2.4576).
CLK1/P	Clock 1 — pulse from TCB clock CLK/P to VMB connector J7 to synchronize DMA operation.
CLK2/P	Clock 2 — pulse from TCB clock to synchronize CTC and surface scan samples.
CONTINUE	Continue — from pseudo-control panel to continue CPU operation at point where it was interrupted by depression of HALT button.
CORSEL/L	Correction switch select — from I/O decoder to enable X or Y correction DIP switch pack data onto low data bus.
CTCSEL/L	Counter timer circuit select — from I/O decoder to accept or output data on low data bus.
DIAG/L	Diagnostic mode — from pseudo-control panel to select ROM 4 (diagnostic mode) instead of ROM 1 at addresses 0 though 7FF (hex).
DIALED/L	Diagnostic LED — from diagnostic flip-flop (affected by RESET, DIASEL or DIAG) to indicate that the TCB is in diagnostic mode.
DIASEL/L	Select diagnostic versus system ROM — from I/O decoder to clock bit 0 of high data bus into flip-flop 2K to select either system ROM (HDB0=H) or diagnostic ROM (HDB0=L).
DMAON/H	Direct memory access on — from VMB to indicate that the VMB is performing direct memory access operation to display text. CPU performs puck-trading measurements only when DMAON is low.

DR/N	Data ready — from CPU (HDB0) to parallel output port to indicate that coordinate data is ready at the coordinate output latches.
DSR/L	Data set ready — PCI status register bit indicating to the CPU that the VGU is busy (H) or done (L).
DTR/L	Data terminal ready — output from PCI used to indicate that the TCB is ready to receive VGU data. DTR turns off IAMBUSY when high.
EXTCLR/N	External clear — input to parallel output port.
FLAG1:FLAG3/H	FLAG (1:3) — control information from CPU (HDB <5:7>) to the parallel output port.
FPB1:FPB8/L	Function pad buttons — from function pad (ICU) to carry function pad button data onto low data bus when selected by FPSEL.
FPD1:FPD4/L	Function pad diodes — from CPU over high data bus to function pad (ICU) LEDs via latch 9D.
FPMUX0:FPMUX7/L	Function pad multiplexer — from function pad (ICU) to carry function pad switch data onto low data bus when selected by FPSEL.
FPSEL/L	Function pad select — from I/O decoder to enable function pad (ICU) data onto low data bus to CPU.
GROUP0:GROUP3/H	Group <0:3> — from CPU (HDB<4:7>) via latch 5L to select one of the 16 groups of surface wires on the tablet.
HALT/L	Halt — from pseudo-control panel to interrupt CPU.
HDBOFF/L	High data bus off — impedes data flow from CPU onto high data bus.
HDB0:HDB7/H	High data bus <0:7> — unidirectional tristate bus connecting the CPU with the indicator light and LED latches, sample control latch, wire select latch, and parallel output circuit.
IAMBUSY/L	I am busy — busy signal sent by TCB to VGU to inhibit data transfer from VGU to TCB.
INDSEL/L	Indicator light select — from I/O decoder to enable HDB0:7 to be displayed on LEDs by latch 9C.
INH/N	Inhibit — input to parallel output port.
INIT/N	Initialize — from CPU (HDB1) to provide an initialize signal at the parallel output port.
INT/L	Interrupt request — from I/O devices to indicate to the CPU that the device needs service.
IORQ/L	Input/output request — from CPU to indicate that the low order byte of the address bus (A <0:4>) holds a valid I/O address for an I/O read or write operation. Also indicates that an interrupt response vector can be placed on the data bus when an interrupt is being acknowledged (with M1).
IPLERR/H	Current pulse error — indicates to CPU that a current ramp has been commanded but did not occur. Set high by RSTINT at start of a wire sample. Set low by presence of surface current at falling edge of STRAMP.
IPLOFF/H	Current pulse off — from the IPLOFF flip-flop 10L (clocked set by the IPLOFF comparator 10N when it senses that current has been on for more than 20 μsec) to disable the group select decoder 2L, shutting off current to the surface. Also sends a reset pulse to the CPU.
IPULS/A	Current pulse select — from current ramp generator to transistor switches. This is the wire pulse to the surface PC board.
KBDRDY/H	Keyboard ready — from PIO to indicate that the A port is empty and ready to receive data.
KBDSTB/N	Keyboard strobe — from keyboard to load data on keyboard bus (KBD 0:7) into PIO A port.
KBD0:KBD7/H	Keyboard bus <0:7> — unidirectional tristate bus that is the data from keyboard to PIO.
LKB0:LDB7/H	Low data bus — bidirectional, tristate bus connecting the CPU with its memories and peripherals.

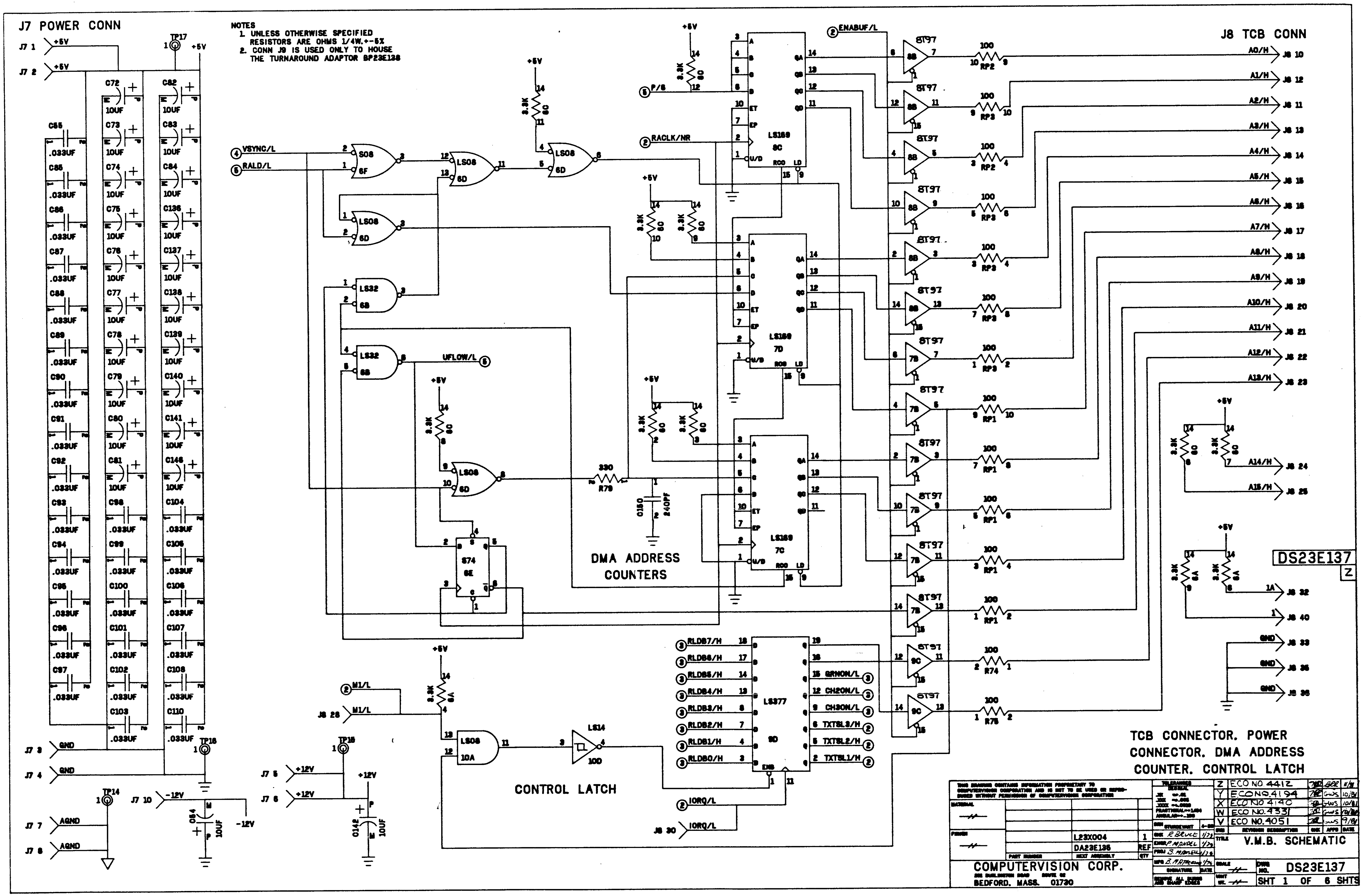
LEDSEL/L	LED select — from I/O decoder to enable HDB0:7 to be displayed on the function pad (ICU) and stylus.
M1/L	Machine cycle 1 — from CPU to indicate that the current machine cycle is the operation code fetch cycle of an instruction execution. Also occurs with IORQ to indicate an interrupt acknowledge cycle. Used as a synchronization pulse to control certain CTC and PIO operations. Also used by DMA logic on VMB.
MREQ/L	Memory request — indicates that the address bus holds a valid address for a memory read or write operation. Generated by the CPU and by the DMA logic on the VMB.
NMI/L	Non-maskable interrupt — causes CPU to go to location 0066_{16} for NMI service routine.
PCICLK/P	Programmable communications interface clock — clocks the PCI receiver, transmitter and busy flip-flop. Generated by channel 1 of the CTC (approximately 76.8 kHz).
PCISEL/L	Programmable communications select — from I/O decoder to enable the PCI. Indicates that data lines to PCI are valid for write operation, or enables PCI to put status or data onto the LDB for a read operation.
PDSSEL/L	Puck and DIP switch select — from I/O decoder to enable LDB 0:7 to carry DIP switch contents (location 8A) to CPU.
PIOSEL/L	Parallel input/output controller select — from I/O decoder to enable PIO to accept data bus contents or to output onto the data bus (LDB).
PROX/L	Proximity — control information from CPU (HDB1) to parallel output port.
PTRRDY/L	Printer ready — from PIO to indicate that B-port register is full and ready to output data.
PRTSTB/N	Printer strobe — to PIO from printer to acknowledge that data has been accepted by the printer.
PTR0:PTR7/H	Printer <0:7> — unidirectional buffered bus that transfers data from the PIO B port to the printer.
PUKD1,PUKD2, PUKD4/L	Puck indicator LEDs — from CPU (HDB) to stylus LEDs, to turn on and off the LEDs.
PUKSIG/A	Puck signal — from stylus, used to calculate digitize position.
PUKS1:PUKS5/L	Puck switches <1:5> — from stylus switches to CPU to indicate stylus switch positions.
RAMSEL/L	RAM select — from memory decoder (produced by A14/H and A15/H both high, or RFSH); gated with MREQ to produce the row address strobe (RAS) to the RAM.
RANGE/H	Range — control information from the CPU (HDB0) to the parallel output port.
RAS/N	Row address strobe — from gated RAMSEL and MREQ signals to strobe row address from memory address multiplexer into RAM.
RDVDAT/H	Receiver data — serial data input to PCI receiver register from VGU.
RD/L	Read — enables data strobed out of RAM onto low data bus (<0:7>). Transfers data from PIO, CTC and PCI to CPU (with other signals) via the low data bus. Clocks parallel output data onto low data bus (7,0:2) to CPU. Activated by CPU and by VMB DMA logic.
RESET/L	Reset — from psuedo-control panel or signal (IPLOFF) to reset the CPU, CTC, PCI and ROM-select flip-flop. Forces the PC in the CPU to zero and initializes the CPU. CPU address and data busses are forced to a high-impedance state, control signals are inactive, and refresh does not occur during reset time.
RFSH/L	Refresh — indicates that the lower 7 bits of the address bus contain a refresh address (originates at the CPU).
RMTGR/N	Remote trigger — external control signal to the parallel output port, transferred to the CPU via LDB 7.
ROMOFF/L	ROM off — from expansion port (VMB) to disable ROMs when an external program is being used (usually inactive).
ROM1SL:ROM4SL/L	ROM 1:4 select — from ROM address decoder to enable ROM specified by A <11:12>.
RSTINT/L	Reset integrator — controls the FET which resets the integrate and hold circuit to zero volts.
RTS/L	Request to send — from PCI to force IAMBUSY active to the VGU (controlled by TCB CPU).

RXRDY/L	Receiver ready — indicates that PCI reciever holding register has data for CPU. Goes inactive when data is read.
SAMP/L	Sample — controls the integrate and hold input gate. A low closes the switch to allow integration to occur; a high opens the switch to cause the integrate and hold op amp to hold its current value until RSTINT or STSAMP occurs.
SCSEL/L	Sample control latch select — from I/O decoder to clock into sample control latch data for addressing and sampling wires.
STOP/L	Stop — from VMB to hold clock CLK/P low (used by VMB DMA circuitry).
STRAMP/H	Start ramp — controls current ramp. A high causes the current pulse to occur; a low resets the current ramp generator.
TRDATA	Transmitter data — serial data from PCI transmitter to VGU.
URBUSY	You are busy — busy signals sent by VGU to TCB to synchronize data transfer, and so that data is sent to VGU only when VGU is ready.
WAIT/L	Wait — a synchronization signal that indicates to the CPU that the addressed memory or I/O device is not ready for data transfer (normally inactive).
WIRSEL/L	Wire select — from I/O decoder to clock into wire address latch the address of surface wire to be sampled.
WR/L	Write — clocks low data bus data from CPU into RAMs; clocks indicator and LED information on high data bus into latches; enables data from CPU on low data bus into PCI; clocks data on high data bus into sample control, wire select, and coordinate output latches.
XAXIS/L	X axis — from sample control latch (HDB0) to select the X axis or Y axis wire groups.
XCOR0:XCOR7	X axis correction <0:7> — from X axis DIP switches onto the low data bus to provide correction factors for coordinate determination routines.
XOVFL/H	X overflow — control bit from CPU (HDB3) to parallel output port.
YCOR0:YCOR7	Y axis correction <0:7> — from Y axis DIP switches onto low data bus to provide correction factors for coordinate determination routines.
YOVFL/H	Y overflow — control information from CPU (HDB4) to parallel output port.
ZAXIS/L	Z axis — control from CPU (HDB2) to parallel output port.
04SEL/L	Select address 4 — enables lower byte of the X coordinate of the stylus (HDB<0:7>) at the parallel output port.
05SEL/L	Select address 5 — from I/O decoder to enable high-order byte of X coordinate at the parallel output port.
06SEL/L	Select address 6 — from I/O decoder to enable the low-order byte of the Y coordinate of the stylus at the parallel output port.
07SEL/L	Select address 7 — from I/O decoder to enable the high-order byte of the Y coordinate of the stylus at the parallel output port.
08SEL/L	Select address 8 — from I/O decoder to enable control information at parallel output port.
09SEL/L	Select address 9 — from I/O decoder to output DR, INIT and BUSY to the parallel output port; gated with RD to enable control information bits (HDB 7,0:2) onto low data bus from output port.

Video Mixer Board



Video Mixer Board Simplified Block Diagram


J7 POWER CONN
NOTES
1. UNLESS OTHERWISE SPECIFIED RESISTORS ARE OHMS 1/4W.+-5%
2. CONN J9 IS USED ONLY TO HOUSE THE TURNAROUND ADAPTOR BP23E138
J8 TCB CONN
DMA ADDRESS COUNTERS
CONTROL LATCH
LS169
LS377
LS08
LS32
S74
LS14
8T97
VSYNC/L
RALD/L
UFLOW/L
ENABUF/L
P/S
RACLK/NR
M1/L
IORQ/L
RLDB7/H
RLDB6/H
RLDB5/H
RLDB4/H
RLDB3/H
RLDB2/H
RLDB1/H
RLDB0/H
GRNON/L
CH2ON/L
CH3ON/L
TXTSL3/H
TXTSL2/H
TXTSL1/H
A0/H
A1/H
A2/H
A3/H
A4/H
A5/H
A6/H
A7/H
A8/H
A9/H
A10/H
A11/H
A12/H
A13/H
A14/H
A15/H
DS23E137
Z
TCB CONNECTOR, POWER CONNECTOR, DMA ADDRESS COUNTER, CONTROL LATCH
Z ECO NO 4412
Y ECO NO 4194
X ECO NO 4140
W ECO NO 4331
V ECO NO 4051
L23X004
DA23E135
V.M.B. SCHEMATIC
COMPUTERVISION CORP.
BEDFORD, MASS. 01730
DS23E137
SHT 1 OF 6 SHTS

HSYNC CONVERTER

HSYNC COUNTER

DMA F/F

DMA TIMING LOGIC

TEXT LINE COUNTERS

TEXT LINE COUNTERS
HYSYNC COUNTER
DMA TIMING LOGIC
HYSNC CONVERTER

DS23E137
Z

SEE SHEET 1

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V.M.B. SCHEMATIC

DWG NO. DS23E137

SHT 2 OF 6 SHTS

RAMA0/H-RAMA7/H
RAMB0/H-RAMB7/H
TEXT RAMS
TEXT LATCH
93422 9E
93422 9G
93422 9F
93422 9H
S374 9J
LATCH/N
ROWAD0/H
ROWAD1/H
ROWAD2/H
ROWAD3/H
5X7 CHAR GEN
3636-1
9K
GRAPHICS/TEXT F/F
LS74 7L
S299 8J
PAR. TO SER. CONV.
DOTCLK/NR
P/7
RESET/L
GRAPH/L
VIDOFF/H
TXTON/H
RAMBWE/N
P/2
RAMBOE/L
RAMAWE/N
RAMAOE/L
RLDB0/H-RLDB7/H
LOADPS/H
CH3ON/L
CH2ON/L
GRNON/L
CH3DOT/H
CH2DOT/H
GRNDOT/H
DS23E137
Z

TEXT RAMS
CHARACTER GENERATOR AND
SHIFT REGISTER SCHEMATIC

SEE SHEET 1

V.M.B. SCHEMATIC

DWG NO. DS23E137

SHT 3 OF 6 SHTS

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LINE RATE DETECTOR

LINE RATE F/F

FREQ. ADJ.
SEE NOTE 1

30 MHZ OSCILLATOR

HOR. SYNC STRIPPER

VERT. SYNC STRIPPER

NOTES:
1. FREQUENCY ADJUSTMENT COIL L1 MUST BE TUNED FOR AN OSCILLATOR FREQUENCY OF 30 +/- .01 MHZ AT ROOM TEMPERATURE AT TP19 OR TP18.

DS23E137
Z

30 MHZ OSCILLATOR AND DIVIDER
SYNC SEPERATOR
LINE RATE DETECTOR

SEE SHEET 1

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TITLE V.M.B. SCHEMATIC

DWG NO. DS23E137

SHT 4 OF 6 SHTS

DOT (÷ 8) COUNTER

TEXT RAM ADDRESS COUNTERS

CHARACTER COUNTER

RAM OUTPUT ENABLE F/F

TEXT ON F/F

RAM BANK SELECT CIRCUIT

SEE NOTE 1

NOTES:

1. LATCH/N - WHEN USING 2102 RAMS, CUT ETCH BETWEEN E1 AND E2. THEN ADD A JUMPER BETWEEN E3 AND E2. REMOVE JUMPERS 8E-5 TO 5E-10 AND 6E-13 TO 5E-11. RESTORE CONNECTION BETWEEN 8E-5 AND 6G-11.

DS23E137 Z

TEXT RAM ADDRESS COUNTERS
TEXT DOT COUNTER
CHARACTER COUNTER
DMA AND DISPLAY LOGIC

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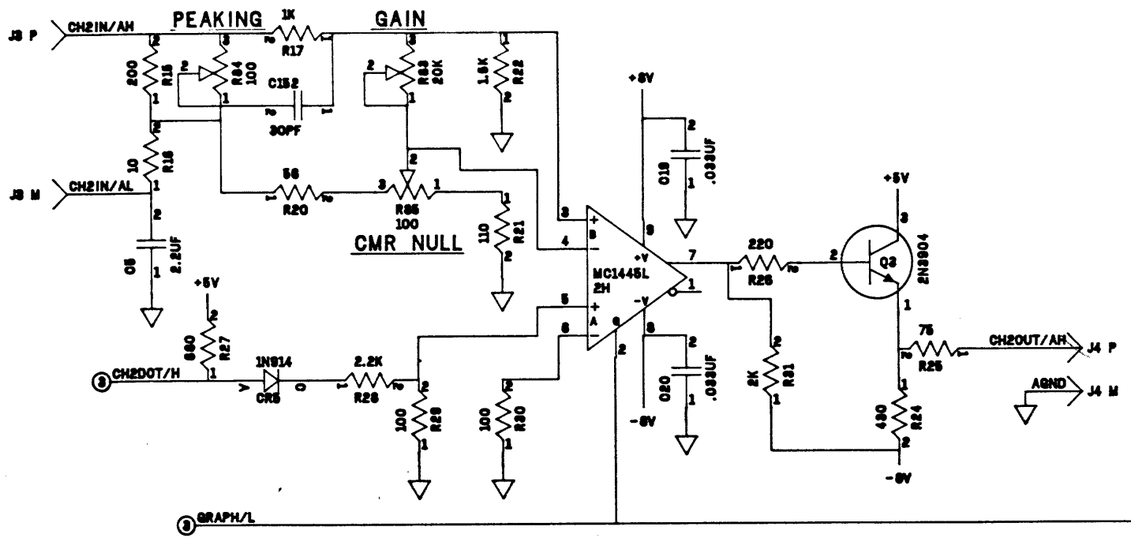
SEE SHEET 1

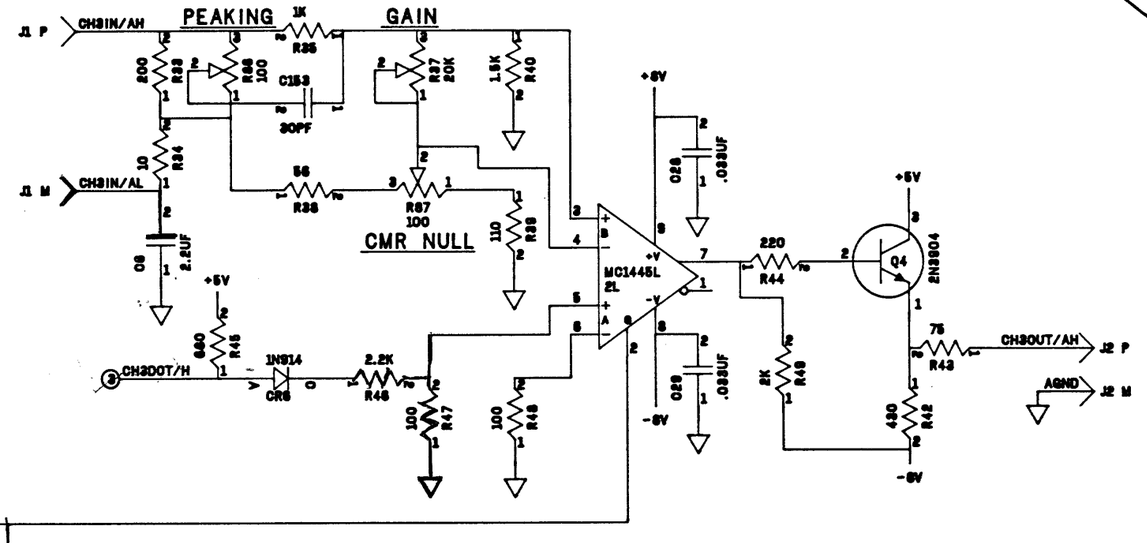
V.M.B. SCHEMATIC

DWG NO. DS23E137

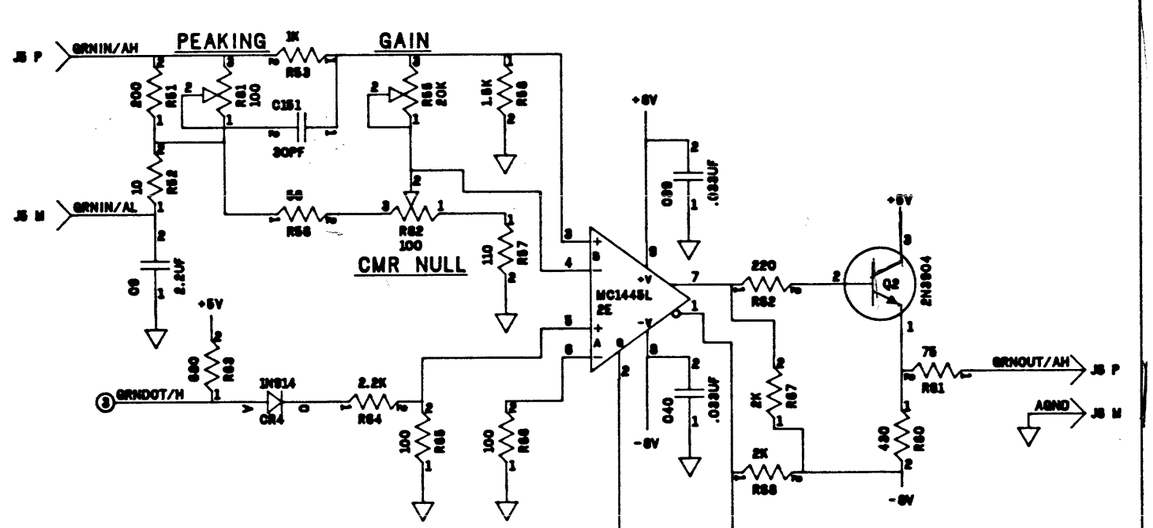
SHT 5 OF 6 SHTS



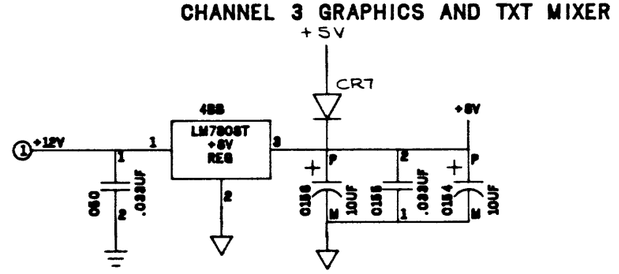
CHANNEL 2 GRAPHICS AND TXT MIXER



CHANNEL 3 GRAPHICS AND TXT MIXER



GREEN (WHITE) GRAPHICS AND TXT MIXER



+8V REGULATOR

-8V REGULATOR

SPARE GATES		
TYPE	LOCATION	QTY
74S04	5E	1
74S08	10K	2
74LS14	10D	3
74123	5L	1

DS23E137
Z

GRAPHICS AND TEXT MIXERS

SEE SHEET 1

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SEE SHEET 1

TITLE V.M.B. SCHEMATIC

DWG NO. DS23E137

SHT 6 OF 6 SHTS

VMB SIGNAL GLOSSARY

A<0:15>/H	Address — unidirectional address bus from DMA address counters to TCB RAMs.
A7/H	Address bit 7 — enable signal for control latch.
BLUDOT/L	Blue dot — from dot gating logic to produce blue dots.
BLUIN/AH	Blue in — video input from VGU to graphics/text mixer.
BLUON/L	Blue on — from Z80 microprocessor (LDB<4>) to gate blue dots to text mixer.
BLUOUT/AH (BLUOUT/AL)	Blue out — Video output from VMB to monitor.
BUSOFF/L	Bus off — from DMA logic to tristate the TCB address bus and control lines.
CLAMP/H	Clamp — black clamp output that suppresses DC offset built up in coupling capacitors during a horizontal line.
CLKAB/N	Clock A and B RAMs — produced by CLKI when MREQ is active and DMA flip-flop is set. CLKAB Resets the "I want the busses" flip-flop and produces RACLK.
CLK1/P	Clock 1 — from TCB system clock to enable STOP and RD signals and produce DMA clock pulse (CLKAB and RACLK).
CTXOFF/L	Communication text off — from Z80 microprocessor (LDB<1>). Addresses VMB ROM to indicate that no communication text is to be displayed.
CURSOR/H	Cursor — from text RAM (bit 7, MSB) via text latch to produce dots for text cursor.
CV/AL	Composite video — video signal from text mixer to sync stripper.
DMAON/H	Direct memory access on — from VMB ROM to initiate DMA transfer. Also informs TCB that DMA is in progress.
DMAST/L	DMA start — from horizontal sync counter to set "enable I want the busses" flip-flop. DMAST synchronizes the first DMA transfer of each field in time for the beginning of the active video area.
DOT/L	Dot — from parallel-to-serial converter to create text characters on the CRT.
DOTCLK/NR	Dot clock — from oscillator to clock text dots out of parallel-to-serial converter.
ENABUF/L	Enable buffers — from DMA logic to enable DMA address onto address bus.
EXSYNC/H	External synchronization — from oscillator logic to synchronize VMB with external signal.
FOUR/L	Four lines — from Z80 microprocessor (LDB<0>). Addresses VMB ROM to indicate that only four lines of communication text are to be displayed.
GRAPH/L	Graphics — from graphics control logic to control text mixer output.
GRNDOT/L	Green dot — from dot gating logic to produce green dots.
GRNIN/AH (GRNIN/AL)	Green in — video input from VGU to graphics text mixer.
GRNON/L	Green on — from Z80 microprocessor (LDB<5>) to gate green dot to text mixer.
GRNOUT/AL (GRNOUT/AH)	Green out — video output from VMB to monitor.
HDBOFF/L	High data bus off — from DMA logic to tristate TCB high data bus.
HLR/H	High line rate — from line rate detector to define the line rate.
HLR/L	High line rate — performs the same functions as HLR/H.

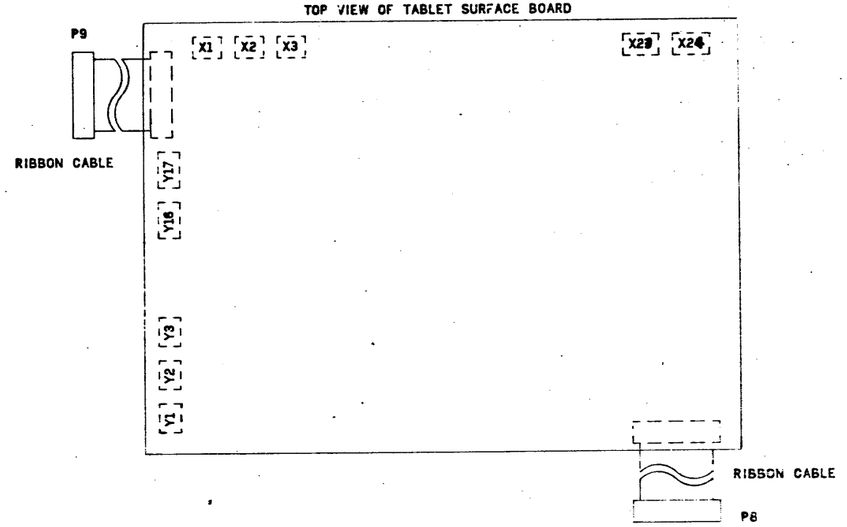
HOR/N	Horizontal — from sync stripper to synchronize VMB logic with the beginning of each scan line.
HOR1/P	Horizontal 1 — from sync stripper to synchronize VMB logic with the beginning of each scan line.
HYSNC/L	Horizontal synchronization — from horizontal sync converter to synchronize VMB logic with the beginning of each scan line.
IORQ	Input/output request — from Z80 microprocessor to clock the control latch and the DMA flip-flop.
IWTB/H	I want the busses — generated by DMA logic to produce signals (HDBOFF, BUSOFF, STOP) that tristate TCB busses and stop TCB clock for DMA transfers.
LATCH/N	Latch — from dot counter to clock text character into text latch every eights dots. LATCH also clocks the text RAM address counters, character counter and text-on flip-flop. LATCH is inverted to LOADPS/H to load the parallel-to-serial converter.
LDB<0:7>/H	Low data bus — unidirectional bus that carries text data to VMB text RAMs and control data to control latch.
LOADPS/H	Load parallel-to-serial converter — inverse of LATCH/N; clocks text character into parallel-to-serial converter and enables CURSOR/H into text cursor logic.
LRCLK/L	Load RAM clock — produced by DMA logic (CLKAB) to clock text RAM address counters for DMA transfers.
MIORQ/L	Memory or input/output request — produced when either MREQ or IORQ from the TCB are active. Clocks "I want the busses" flip-flop to begin DMA transfer.
MREQ/L	Memory request — from TCB to indicate a memory cycle is in progress. Clocks DMA and "I want the busses" flip-flop. Also produced by VMB to enable DMA clock pulse (CLKAB).
M1/L	Machine cycle 1 — from Z80 microprocessor to indicate that an op code fetch cycle is in progress. Disables control latch and prevents DMA cycles.
RAMA<0:7>/H	RAM A address — unidirectional address bus to text RAM bank A.
RAMAEO/L	RAM A output enable — from RAM output enable flip-flop to strobe data out of RAM bank A.
RAMAWE/N	RAM A write enable — from RAM bank select circuit to strobe data into RAM bank A.
RAMB<0:7>/H	RAM B address — unidirectional address bus to text RAM bank B.
RAMBOE/L	RAM B output enable — from RAM output enable flip-flop to strobe data out of RAM bank B.
RAMBWE/N	RAM B write enable — from RAM bank select circuit to strobe data into RAM bank B.
RACLK/NR	Row address clock — produced by VSYNC or CLKAB to clock the DMA address counters.
RALD/L	Row address load — from DMA logic to load first communication text address into DMA address counters.
RAMOFF/L	RAM off — from character count logic to disable text RAM address counters; K input to text-on flip-flop.
RD/L	Red — from DMA logic to enable TCB RAM data onto low data bus.
REDDOT/H	Red dot — from dot gating logic to produce red text dots.
REDIN/AH (REDIN/AL)	Red in — video input from VGU to graphics text mixer.
REDON/L	Red on — from Z80 microprocessor (LDB<3>) to gate red dot to text mixer.
REDOUT/AH (REDOUT/AL)	Red out — video output from VMB to monitor.
RESET/L	Reset — from Z80 microprocessor to reset DMA flip-flop.
ROWAD<0:3>/H	Row address — from horizontal sync counter to specify the row of dots in each text character that are to be displayed.
STOP/L	Stop — from DMA logic to enable DMA cycle stealing by stopping TCB clock.

STXOFF/L	Status text off — from Z80 microprocessor (LDB<2>). Addresses VMB ROM to indicate that no status text is to be displayed.
TXTLIN/L	Text line — from the horizontal sync counter to indicate the beginning of a new text line (every 13 scan lines).
TXTOFF/L	Text off — from VMB ROM to turn off text as directed by Z80 microprocessor.
UFLOW/L	Underflow — from DMA address counters to indicate that last status text character has been transferred.
VSYNC	Vertical synchronization — from sync stripper to synchronize VMB logic with the beginning of each video field.
1.25 MHz/P	1.25 megahertz — from oscillator logic onto lock horizontal sync converter and internal sync generator.
15 MHz/P	15 megahertz — 15 megahertz clock pulse from oscillator logic for low line rate.
30 MHz/N	30 megahertz — 30 megahertz clock pulse from oscillator; divided to produce 15 megahertz pulse.
30 MHz/P	30 megahertz — 30 megahertz clock pulse that regulates VMB functions.
80CT/L	80 count — from the text RAM address counters to indicate that the 80th DMA transfer (one full text line) is complete.

Tablet Surface Grid Board

	Sheet No.
Y Position Wires	1
X Position wires	2

TOP VIEW OF TABLET SURFACE BOARD



WIRES TO DETERMINE Y POSITION

DS23E112
A

MATERIAL —

FINISH —

PART NUMBER	NEXT ASSEMBLY	QTY
DA23E110		1

TOLERANCES
DECIMAL
XX ±0.01
.XXX ±0.005
.XXXX ±0.0050
FRACTIONAL ±1/64
ANGULAR ±2°

DRN S HOBBS 7-9
CHK C. Bruce 9/5
ENGR
PROJ
MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

STM	REVISION DESCRIPTION	CHK	APPD	DATE
A	REL ECO 3167	RS	BTZ	9/9/9

TITLE TABLET SURFACE SCHEMATIC DIAGRAM

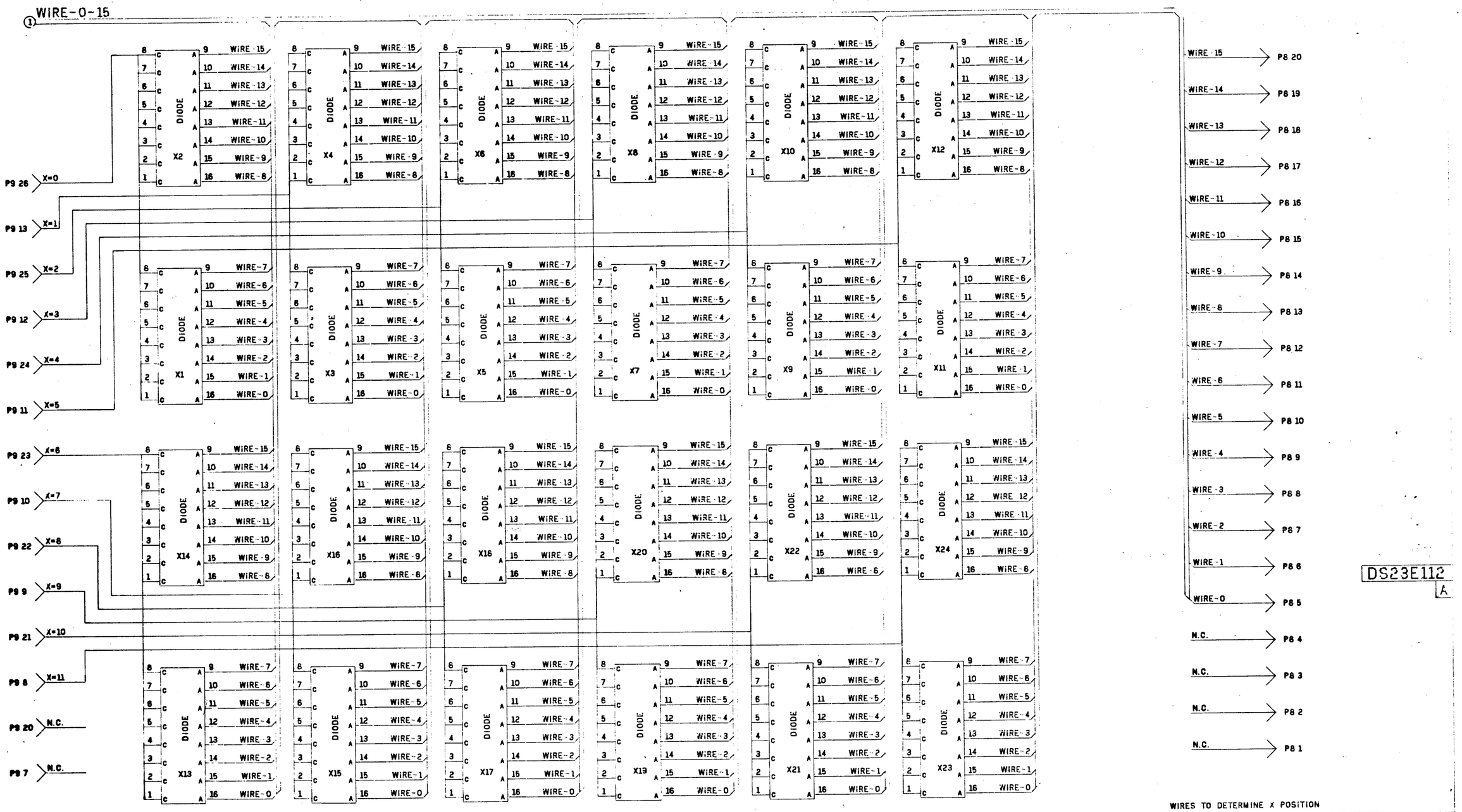
SCALE —

DWG NO. DS23E112

UNIT WT. —

SHT 1 OF 2 SHTS

COMPUTERVISION CORP.
100 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730



THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION

MATERIAL

FINISH

PART NUMBER DA23E110 NEXT ASSEMBLY 1 QTY

TOLERANCES
DECIMAL
XX +-.01
XXX +-.005
XXXX +-.0010
FRACTIONAL +-1/64
ANGULAR +-.1DG

DRN B HOBBS 7-6
CHK
ENGR
PROJ
MFR
SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

SEE SHT 1

SYM	REVISION DESCRIPTION	CHK	APPD	DATE

TITLE TABLET SURFACE SCHEMATIC DIAGRAM

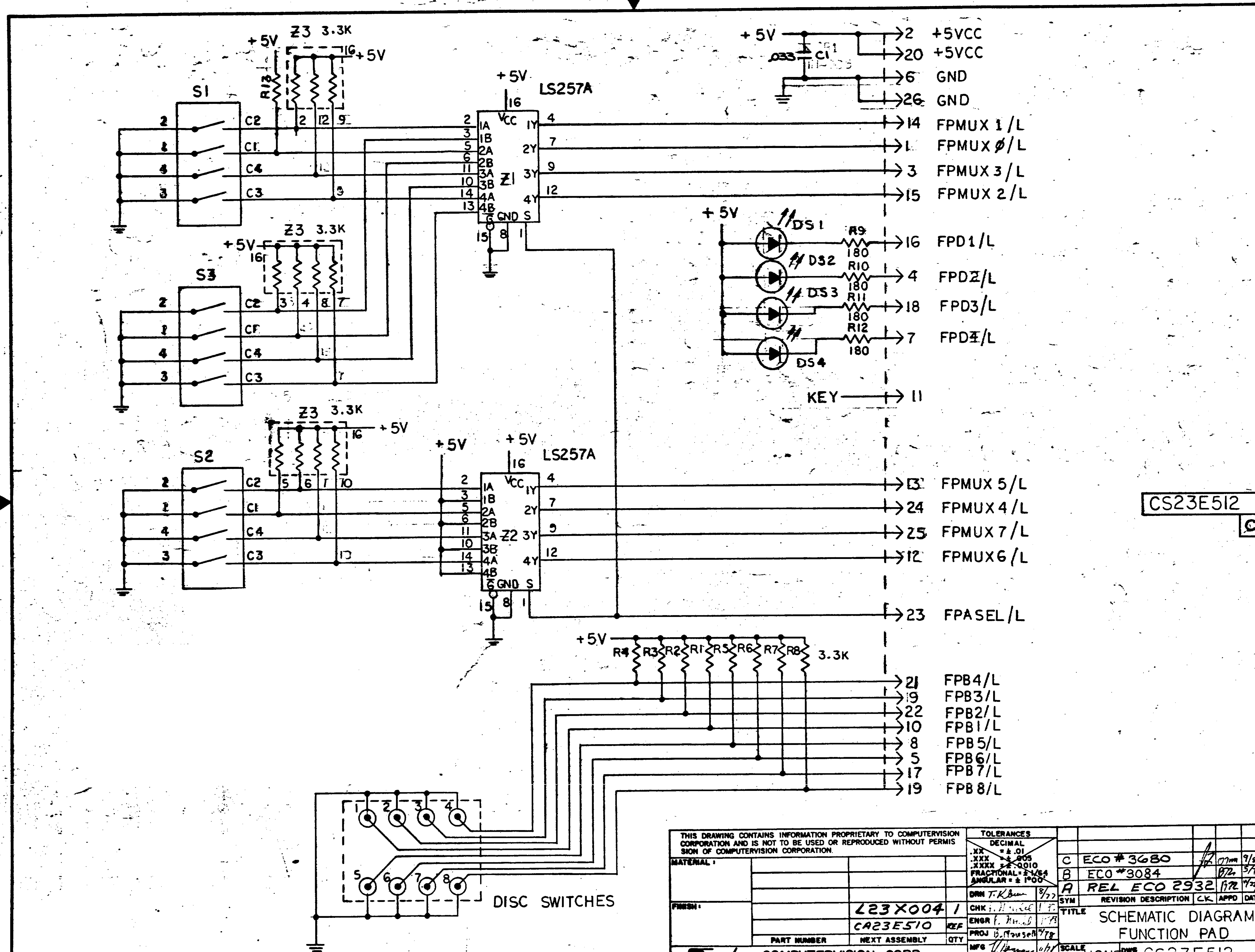
SCALE DWG NO DS23E112

UNIT WT. SHT 2 OF 2 SHTS

COMPUTERVISION CORP.
301 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

Image Control Unit*

*Formerly called the Function Pad



THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.

MATERIAL:		
FINISH:	L23X004	1
	CA23E510	REF
	PART NUMBER / NEXT ASSEMBLY	QTY

TOLERANCES: DECIMAL .XX = ± .01, .XXX = ± .005, .XXXX = ± .0010, FRACTIONAL = ± 1/64, ANGULAR = ± 1°00'

SYM	REVISION DESCRIPTION	CK.	APPD	DATE
C	ECO # 3680			9/80
B	ECO # 3084			5/79
A	REL ECO 2932			

DRN T. K. | CHK | ENGR | PROJ | MFG — SIGNATURE / DATE

TITLE: SCHEMATIC DIAGRAM FUNCTION PAD

SCALE: NONE — DWG NO. CS23E512

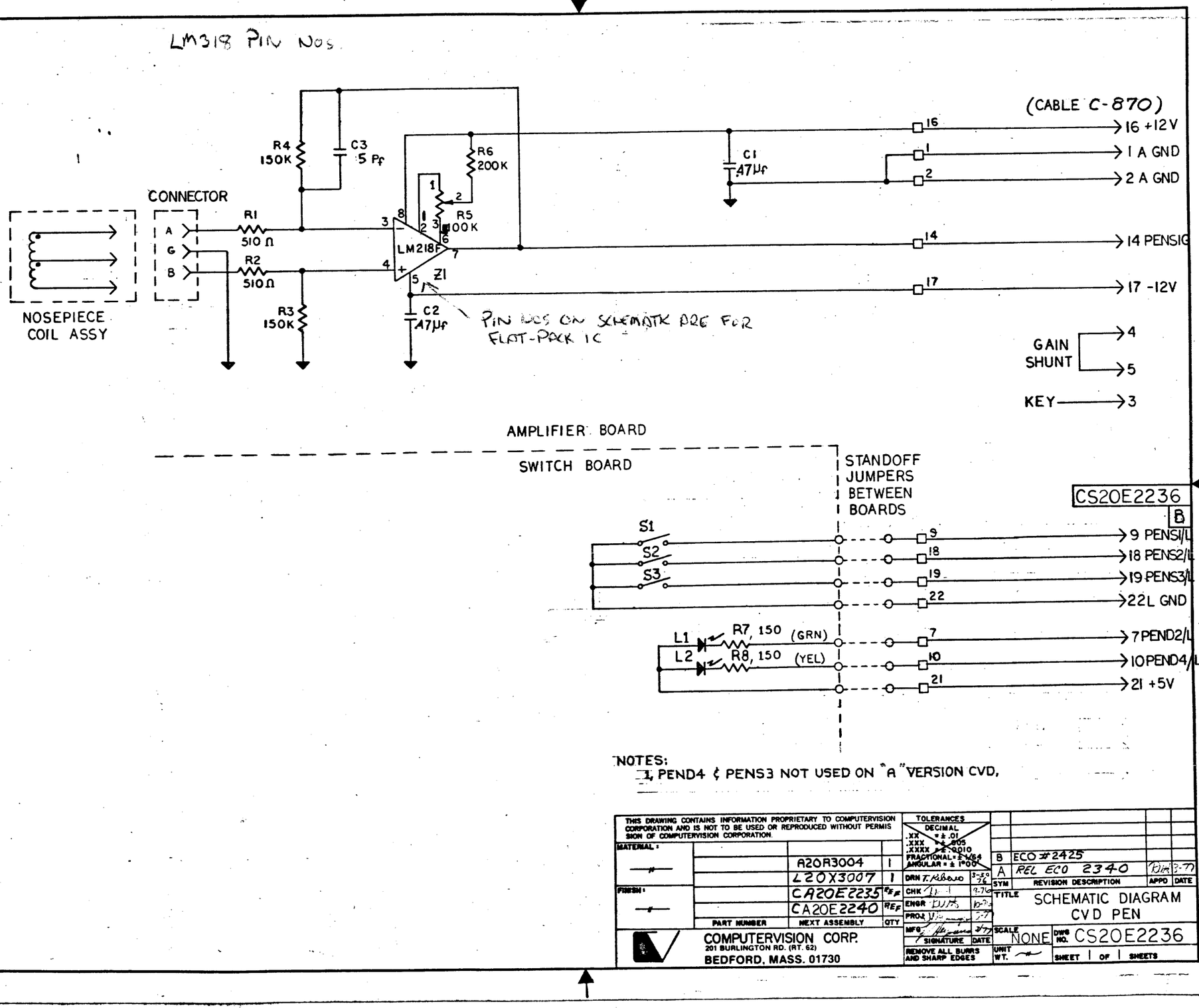
REMOVE ALL BURRS AND SHARP EDGES

UNIT WT. — SHEET 1 OF 1 SHEETS

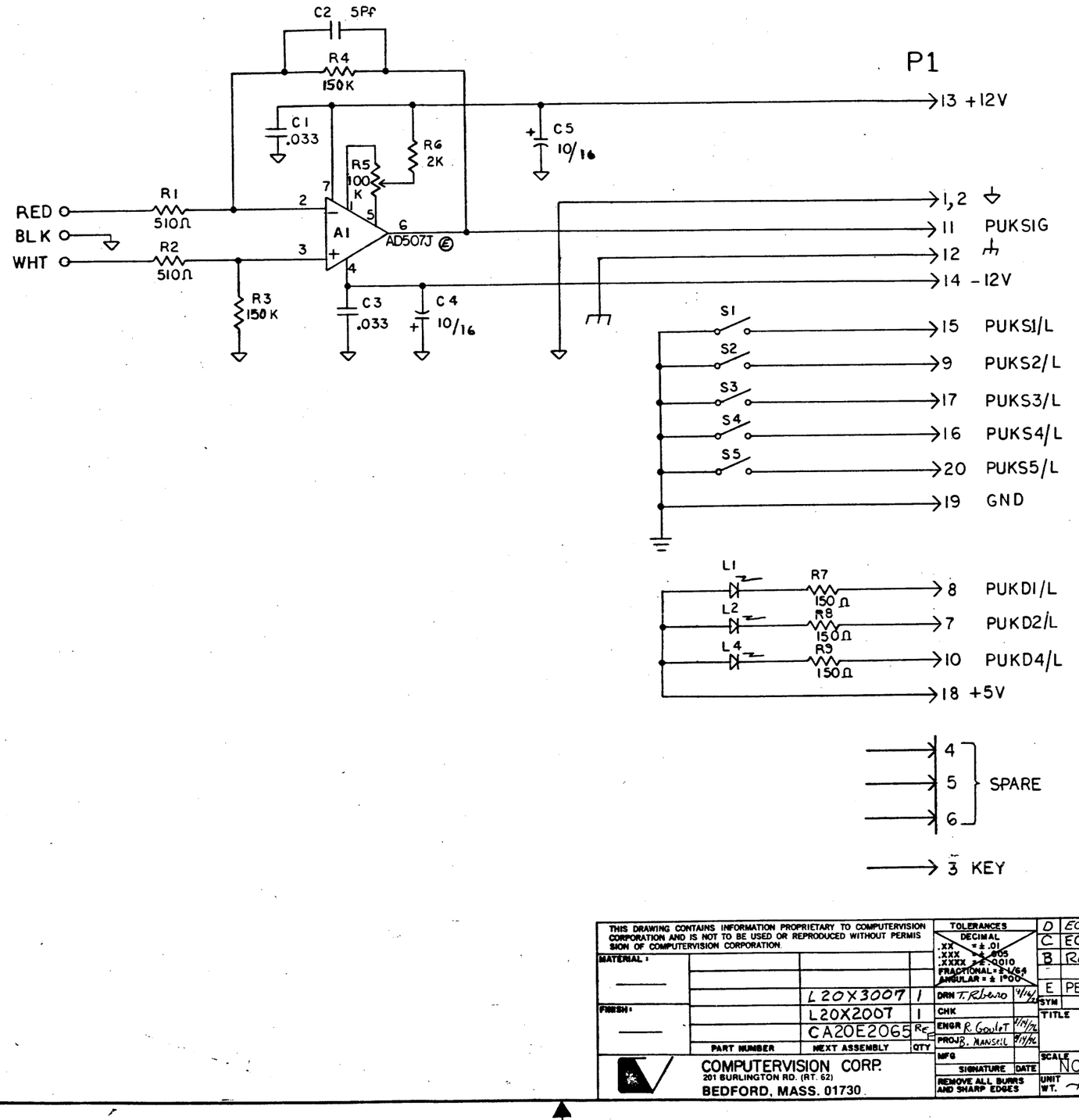
COMPUTERVISION CORP.
201 BURLINGTON RD. (RT. 62)
BEDFORD, MASS. 01730

REV A = REV 3

Pen


LM318 PIN NOS.
(CABLE C-870)
16 +12V
1 A GND
2 A GND
14 PENSIG
17 -12V
GAIN SHUNT
4
5
KEY
3
R4 150K
C3 5 Pf
R6 200K
C1 .47µf
CONNECTOR
A
G
B
R1 510 Ω
R2 510Ω
R5 100K
LM218F
Z1
R3 150K
C2 .47µf
PIN NOS ON SCHEMATIC ARE FOR FLAT-PACK IC
NOSEPIECE COIL ASSY
AMPLIFIER BOARD
SWITCH BOARD
STANDOFF JUMPERS BETWEEN BOARDS
S1
S2
S3
9 PENS1/L
18 PENS2/L
19 PENS3/L
22L GND
L1
L2
R7, 150 (GRN)
R8, 150 (YEL)
7 PEND2/L
10 PEND4/L
21 +5V
CS20E2236
B
NOTES:
1, PEND4 & PENS3 NOT USED ON "A" VERSION CVD.
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION.
MATERIAL:
FINISH:
A20A3004 1
L20X3007 1
CA20E2235 REF
CA20E2240 REF
PART NUMBER NEXT ASSEMBLY QTY
COMPUTERVISION CORP.
201 BURLINGTON RD. (RT. 62)
BEDFORD, MASS. 01730
TOLERANCES
DECIMAL
.XX ± .01
.XXX ± .005
.XXXX ± .0010
FRACTIONAL ± 1/64
ANGULAR ± 1°00
DRN T. Ribeiro 3-30-76
CHK 9-76
ENGR 10-7
PROJ 7-7
MFG
SIGNATURE DATE
REMOVE ALL BURRS AND SHARP EDGES
B ECO #2425
A REL ECO 2340 3-77
SYM REVISION DESCRIPTION APPD DATE
TITLE SCHEMATIC DIAGRAM CVD PEN
SCALE NONE
DWG NO. CS20E2236
UNIT WT.
SHEET 1 OF 1 SHEETS

Puck



CS20E2068

E

PART NUMBER	NEXT ASSEMBLY	QTY
	L20X3007	1
	L20X2007	1
	CA20E2065	REF

MATERIAL: —

FINISH: —

TOLERANCES
DECIMAL
.XX = ± .01
.XXX = ± .005
.XXXX = ± .0010
FRACTIONAL = ± 1/64
ANGULAR = ± 1°00'

	SIGNATURE	DATE
DRN	T. Ribeiro	9/14/82
CHK		
ENGR	R. Goulet	9/14/82
PROJ	B. Mansell	9/14/82
MFG		

REMOVE ALL BURRS AND SHARP EDGES

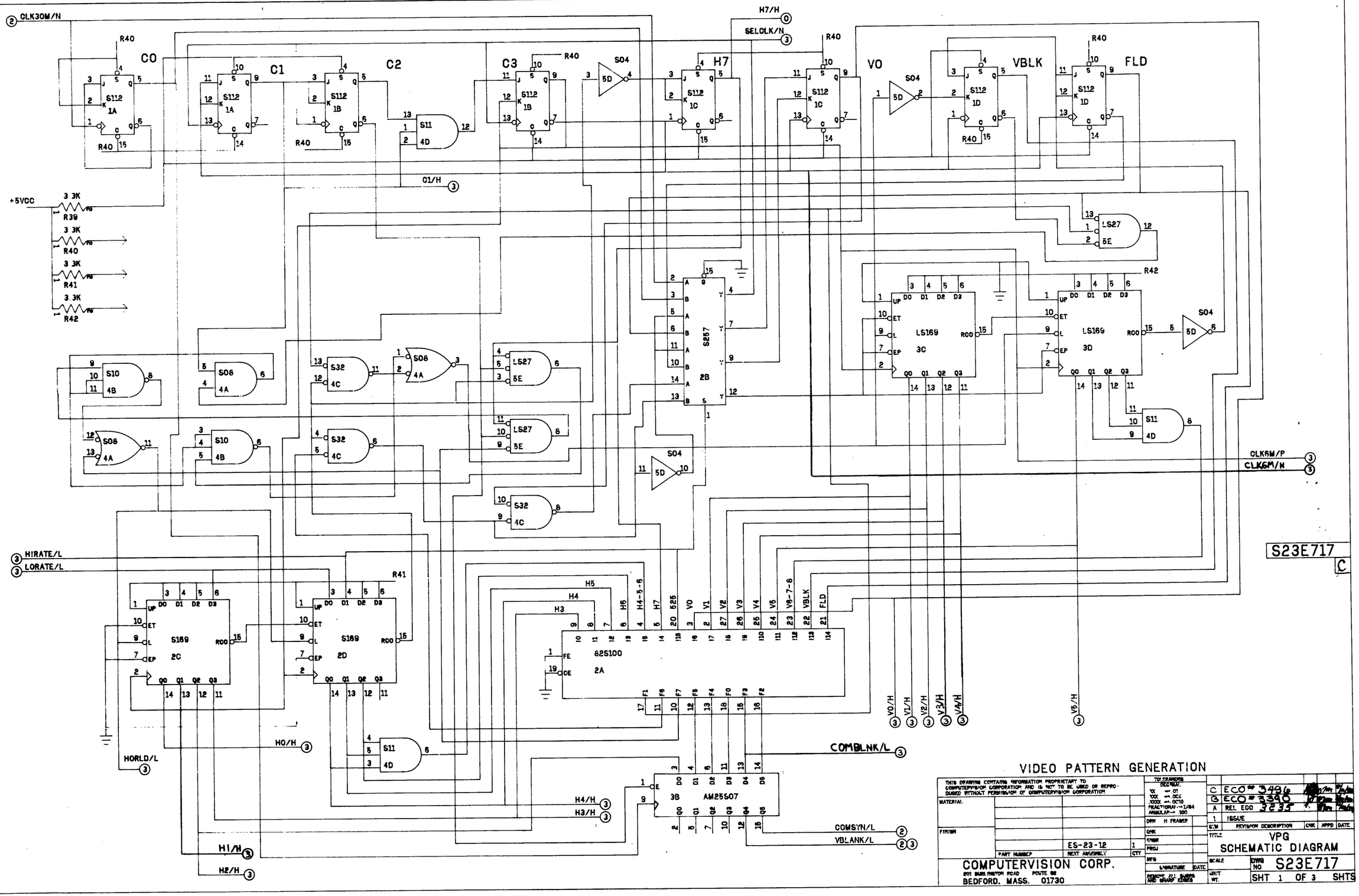
COMPUTERVISION CORP.
201 BURLINGTON RD. (RT. 62)
BEDFORD, MASS. 01730

SYM	REVISION DESCRIPTION	BY	APPD	DATE
D	ECO #2270	—		9-27
C	ECO #2156	—		7/14
B	Release ECO2065	REO		1/29/82
E	PER ECO #2837	KT	JM	9/14/83

TITLE: SCHEMATIC DIAGRAM PUCK

SCALE: NONE
DWG NO. CS20E2068
UNIT WT.
SHEET 1 OF 1 SHEETS

Video Pattern Generator



S23E717

C

VIDEO PATTERN GENERATION

C	ECO # 3496		
B	ECO # 3390		
A	REL ECO 3235		
1	ISSUE		
S/W	REVISION DESCRIPTION	CHK	APPD	DATE

MATERIAL:

FINISH:

PART NUMBER: ES-23-12 NEXT ASSEMBLY: 1 QTY

DRN H FRASER

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

TOP STANDARDS
DECIMAL
XX +-.01
XXX +-.005
.XXXX +-.0010
FRACTIONAL +-1/64
ANGULAR +-.100

REMOVE ALL BURRS AND SHARP EDGES

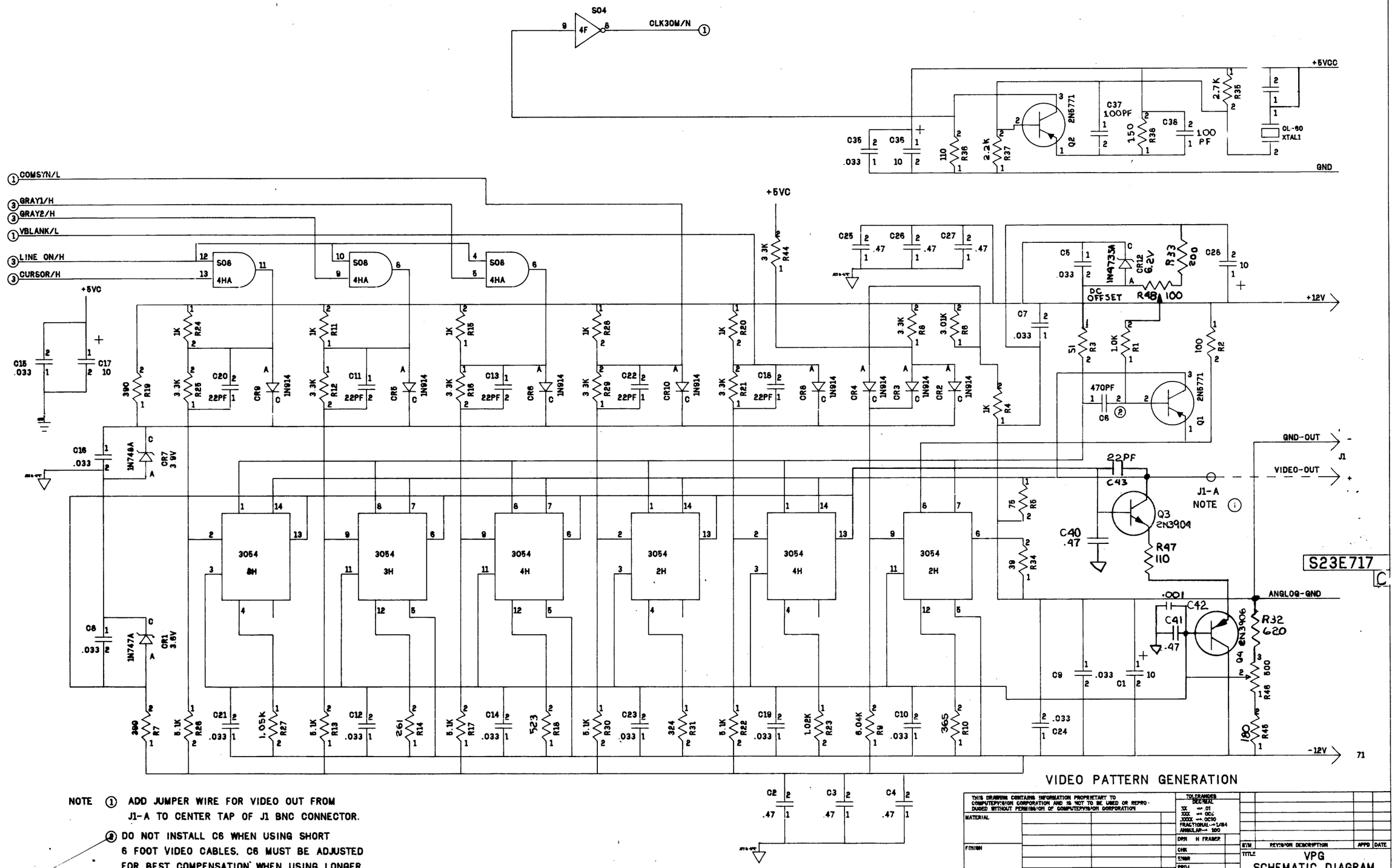
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730

SCALE

UNIT WT.

DWG NO S23E717

SHT 1 OF 3 SHTS



NOTE (1) ADD JUMPER WIRE FOR VIDEO OUT FROM J1-A TO CENTER TAP OF J1 BNC CONNECTOR.

(2) DO NOT INSTALL C6 WHEN USING SHORT 6 FOOT VIDEO CABLES. C6 MUST BE ADJUSTED FOR BEST COMPENSATION WHEN USING LONGER CABLE LENGTHS. VALUE SHOWN IS FOR 1000 FT.

VIDEO PATTERN GENERATION

MATERIAL

FINISH

PART NUMBER | NEXT ASSEMBLY | QTY

TOLERANCES UNLESS SPECIFIED: DECIMAL XX = .01, XXX = .005, XXXX = .0010; FRACTIONAL = 1/64; ANGULAR = 1°

DRN H FRABER

CHK

ENGR

PROJ

MFG

SIGNATURE DATE

REMOVE ALL BURRS AND SHARP EDGES

BY	REVISION DESCRIPTION	APPD	DATE

TITLE VPG SCHEMATIC DIAGRAM

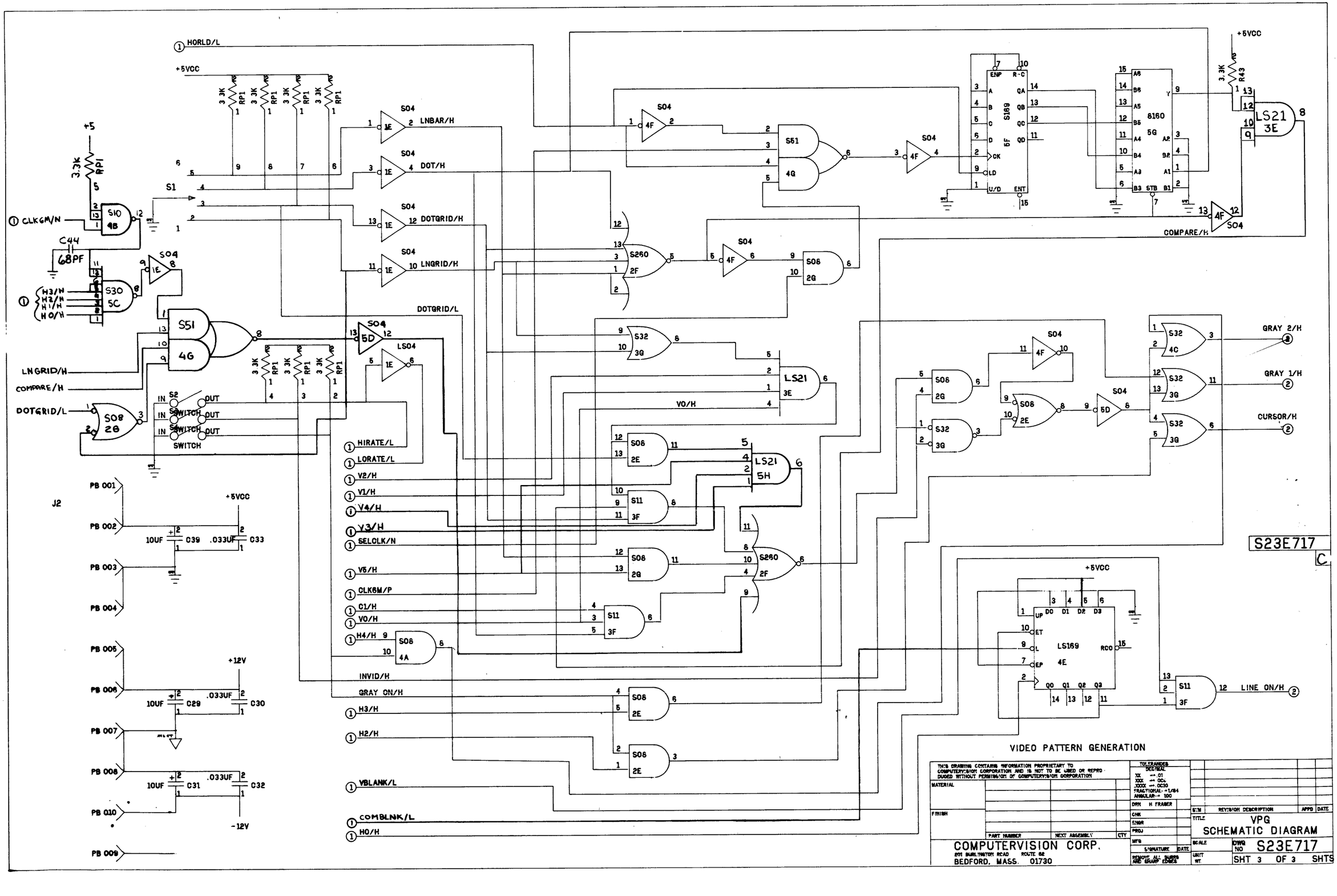
SCALE

DWG NO S23E717

UNIT WT.

SHT 2 OF 3 SHTS

COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730


HORLD/L
+5VCC
3.3K RP1
S04
LNBAR/H
DOT/H
DOTGRID/H
LNGRID/H
S1
+5
CLKGM/N
S10 4B
C44 68PF
S30 5C
H3/H
H2/H
H1/H
H0/H
S51 4G
LNGRID/H
COMPARE/H
DOTGRID/L
S08 2B
S2 SWITCH
IN
OUT
HIRATE/L
LORATE/L
V2/H
V1/H
V4/H
V3/H
SELCLK/N
V5/H
CLK6M/P
C1/H
V0/H
H4/H
S08 4A
INVID/H
GRAY ON/H
H3/H
H2/H
VBLANK/L
COMBLNK/L
H0/H
DOTGRID/L
LS04
S08 5D
S51 4Q
S260 2F
S32 3G
LS21 3E
VO/H
S08 2E
LS21 5H
S11 3F
S08 2G
S08 4A
S08 2E
S08 2E
S11 3F
S08 2E
S08 2E
S169 6F
ENP
ENT
U/D
CK
LD
QA
QB
QC
QD
RC
8160 5G
STB
LS21 3E
+5VCC
3.3K R43
COMPARE/H
S32 4C
S32 3G
S32 3G
S08 2G
S08 2E
S08 2G
S04 5D
GRAY 2/H
GRAY 1/H
CURSOR/H
J2
PB 001
PB 002
PB 003
PB 004
PB 005
PB 006
PB 007
PB 008
PB 010
PB 009
10UF C39
.033UF C33
+12V
10UF C29
.033UF C30
10UF C31
.033UF C32
-12V
+5VCC
LS169 4E
DO D1 D2 D3
UP
CET
CEP
RCO
Q0 Q1 Q2 Q3
S11 3F
LINE ON/H
S23E717
C
VIDEO PATTERN GENERATION
THIS DRAWING CONTAINS INFORMATION PROPRIETARY TO COMPUTERVISION CORPORATION AND IS NOT TO BE USED OR REPRODUCED WITHOUT PERMISSION OF COMPUTERVISION CORPORATION
MATERIAL
FINISH
PART NUMBER
NEXT ASSEMBLY
QTY
TOLERANCES DECIMAL
XX ±.01
XXX ±.005
XXXX ±.0010
FRACTIONAL ± 1/64
ANGULAR ± 100
DRN H FRABER
CHK
ENGR
PROJ
MFG
SIGNATURE
DATE
REMOVE ALL BURRS AND SHARP EDGES
UNIT WT
COMPUTERVISION CORP.
201 BURLINGTON ROAD ROUTE 62
BEDFORD, MASS. 01730
S/M REVISION DESCRIPTION APPD DATE
TITLE VPG SCHEMATIC DIAGRAM
SCALE
DWG NO S23E717
SHT 3 OF 3 SHTS

Please cut along this line

REMARKS FORM

Your comments and suggestions will help us in our continuous effort to improve the quality and usefulness of our publications. All comments and suggestions become the property of Computervision.

TITLE: _____

Order No.: _____

TECHNICAL or EDITORIAL ERRORS (include page number):

SUGGESTIONS FOR IMPROVEMENT:

FROM:
(Please print)

NAME: _____ DATE _____

TITLE: _____

COMPANY NAME _____

ADDRESS _____

CITY _____ STATE _____ ZIP _____

Table of Contents

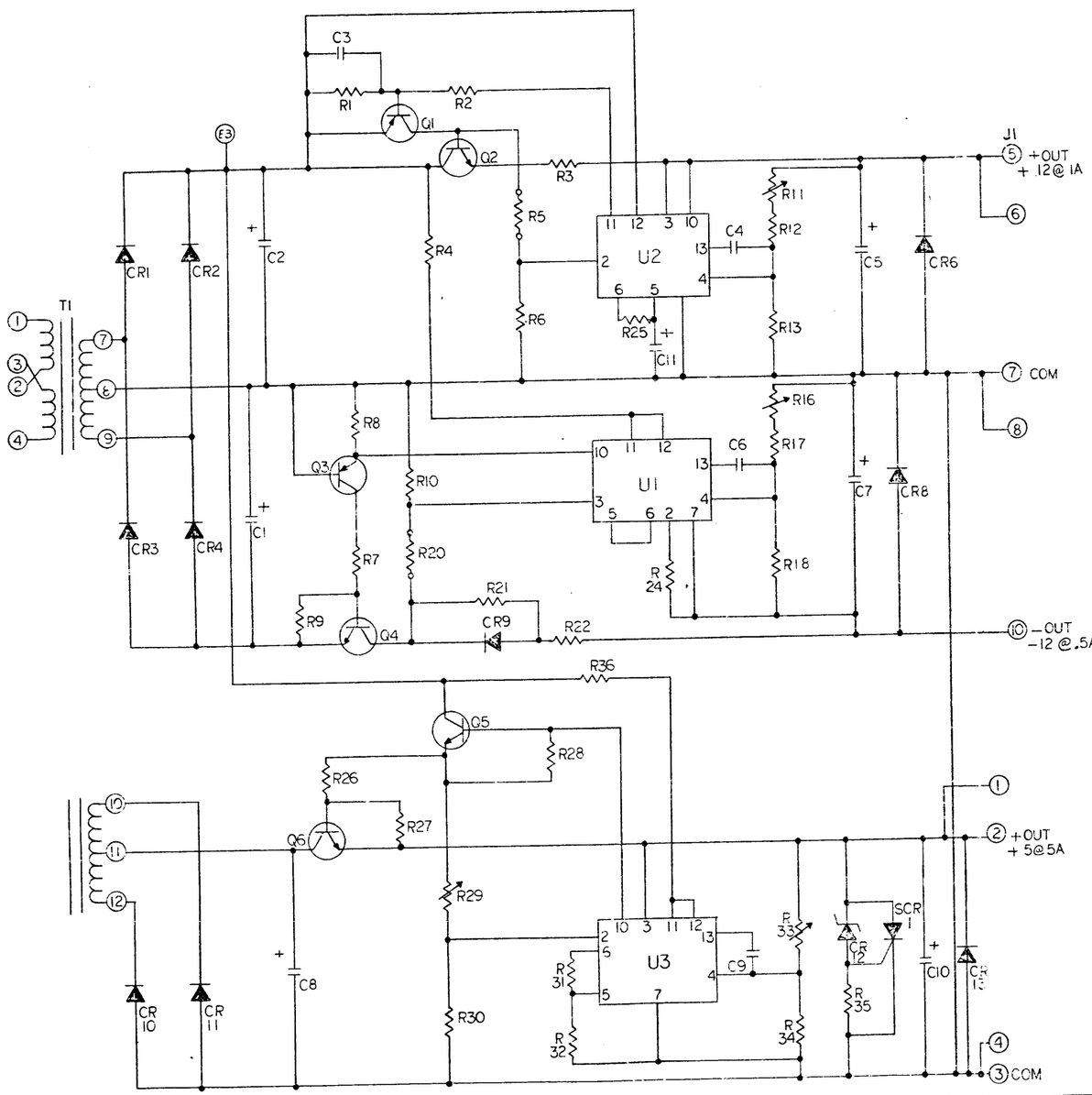
Tablet Power Supply

Keltron: Outline and Schematic

Power-One, Inc: Schematic

Power Supply, Incorporated: Schematic

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	PROTO CLEAN-UP	2/21/79	J.F.
	B	ADDED J1	8-13-79	K.C.
2274	C	C82 WAS 151-10411	10/22/79	KC
2541	D	ADDED NOTE TO SCHEMATIC #6113	12-13-79	KC
4438	E	ADDED HARDWARE LIST	1-14-81	KC



NOTES:

1. RTV LARGE CAPS TOGETHER ON BOARD.

				LAST REFERENCE DESIGNATION USED					CP331
2	360-20018	SLEEVING, 186A, 7/8"	C8+, C8-	C10	CR13	Q6	R35		
1	350-10663	SCREW 6-32 X1"	SCR1	SCR1	T1	U3	E3		
1	402-13920	HEATSINK	SCR1	J1					
2	321-10679	I.C. SOCKET, 14 PIN	U1, U2	NOT USED				NEXT ASSY	USED ON
QTY	STD. P/N	DESCRIPTION	USED ON	R14, R15, R19, R23, CR5, CR7				APPLICATION	
HARDWARE LIST				E1, E2					

	QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	STD P/N
				PARTS LIST	
			C1, 2	2200/35 CAPACITOR ALUM ELECT	102-10100
			C3		101-10110
			C5, 7	100/35	102-10096
2			C8	16000/15	101-10107
			C10	220-16	101-10111
			C11	1/50 ALUM ELECT	104-10093
			C4	.001/100 MYLAR	104-10092
			C6	.003-100	104-10095
			C9	.01/100 CAPACITOR MYLAR	
			CR1, 2, 3, 4, 6, 8, 9	AEIC DIODE 1A 200V	111-10251
			CR10, 11	MR750 22A 50V	111-10256
			CR12	1N752A ZENER	112-10006
			CR13	AF3B DIODE 3A 100V	111-10252
			SCR1	50508LS3 SCR 50V 8A	160-10013
			Q1, 3	2N2907A TRANSISTOR	172-10248
			Q2, 4	12500-3	171-10261
			Q6	12505-2	171-10262
			Q5	2N6551 TRANSISTOR	172-10249
			U1, 2, 3	Lin 723 I C VOLTAGE REGULATOR	130-10287
			R1	1.6K RESISTOR ½W 5% CF	151-10370
			R2, 5, 7, 8, 20, 36	330Ω	151-10353
			R4	750Ω	151-10362
			R6, 9, 10	4.7K	151-10381
			R17, 12	150Ω	151-10345
			R24	47Ω	151-10333
			R21	1.5Ω	151-10302
			R26	2.7Ω	151-10305
			R27	22Ω	151-10325
			R28	2.2K	151-10373
			R25	470Ω	151-10357
			R30	3.9K	151-10379
			R35	82Ω ½W 5% CF	151-10339
			R13, 18	1.2K ½W 2% MF	152-10507
			R32, 31	2.4K	152-10514
			R34	2K ½W 2% MF	152-10512
			R3, 22	.56Ω 2W 10% BWH	158-10082
			R11, 16, 33, 29	2K RESISTOR POTENTIOMETER	154-20020
			J1	1-380991-0 CONNECTOR AMP	901-10823
			T1	16116 TRANSFORMER	082-16116
			PCB	16117 PRINTED CIRCUIT BOARD	505-16117
			CHASSIS	16114 CHASSIS	412-16114

TOLERANCE .XX = .030 .XXX = .010	CONTRACT NO.	POWER-ONE, INC. CAMARILLO, CALIF. 93010 (805)484-2806	
MATERIAL	APPROVALS / DATE: DRAWN J. FOORMAN 6-12-79; CHECKED [illegible]; ENG. APP. [illegible]; APPROVED	TITLE: SCHEMATIC	
FINISH		SIZE: D; CODE IDENT NO.: 54407; DRAWING NO.: 16113; REV: E	
DO NOT SCALE DRAWING		SCALE: —; SHEET 1 OF 1	

8/3/81

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

2N6109 Q101
.0022 1KV C102
VR 101 1K
R 103 8.45K
0.18Ω R105
R 106 47Ω
VR 102 200Ω
P1 5-6 +12V 1A
C104 220 16V
R101 680Ω
1/4 LM 324
R102 47K
2N3904 Q102
D101 D102 1N914B
1N914B D103
R104 2.32K
3.3 50V TANT C103
R107 12K
R108 470K TO FAN +12V
2200 40V C101
COM
2N5883 Q201
.05Ω 3W R206
P1-1-2 +5V 5A
R201 33Ω 1/2W
TIP121 Q202
R202 4.7K
.0047 C202
4.7K R 12
2.21K R204
VR201 1K
1/4 LM 324
1N914B D203
R205 8.43K
C203 33/35V
R 207 47Ω
VR202 200Ω
3.3K R208
1N752A D 204
R209 4.7Ω
1K VR 203
R-210 220
33/10V C204
S2006 LS3
1000 @ 10V C205
R211 130Ω 1/4W
ZN 458 2.45V D12
IN4004 D201
BR252
CR 201
12000 15V C201
CB1
Note
115 VAC Jump 1-2 3-4
230 VAC Jump 2-3
T1
IN4004 D131 D132 D133 D134
2200 40V C301
R301 820Ω
IN754A D301
.0022 C305
R 302 4.7K
200 DE C302
1/2 LM358 A3
R303 100K
4.7K R304
1K VR301
8.45K R305
1/2 LM358
68K R307
33K R310
ZN 3904 Q302
1N914B D303
D302 ZN 458 2.45V
R306 2.32K
VR302 200Ω
R308 47Ω
C309 220 16V
Q301
2N5294
0.18Ω R309
-12V P1-10 0.5A
COM P1-3,4,7-9

ALL COMPONENT VALUES ARE TYPICAL
JUST FOR REFERENCE ONLY

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES	DRAWING STARTED	DATE
	DRAWN HGH	6-15-81
MATERIAL:	CHECKED JLV	6/16/81
FINISH:	ENGR	

Power Supplies, Incorporated
5 Brookside Drive – P.O. Box 447
Middlefield, Connecticut 06455

SCHEMATIC PSI 1170A

SIZE	CODE IDENT NO.	
C	34050	12701

SCALE SHEET

8/3/81